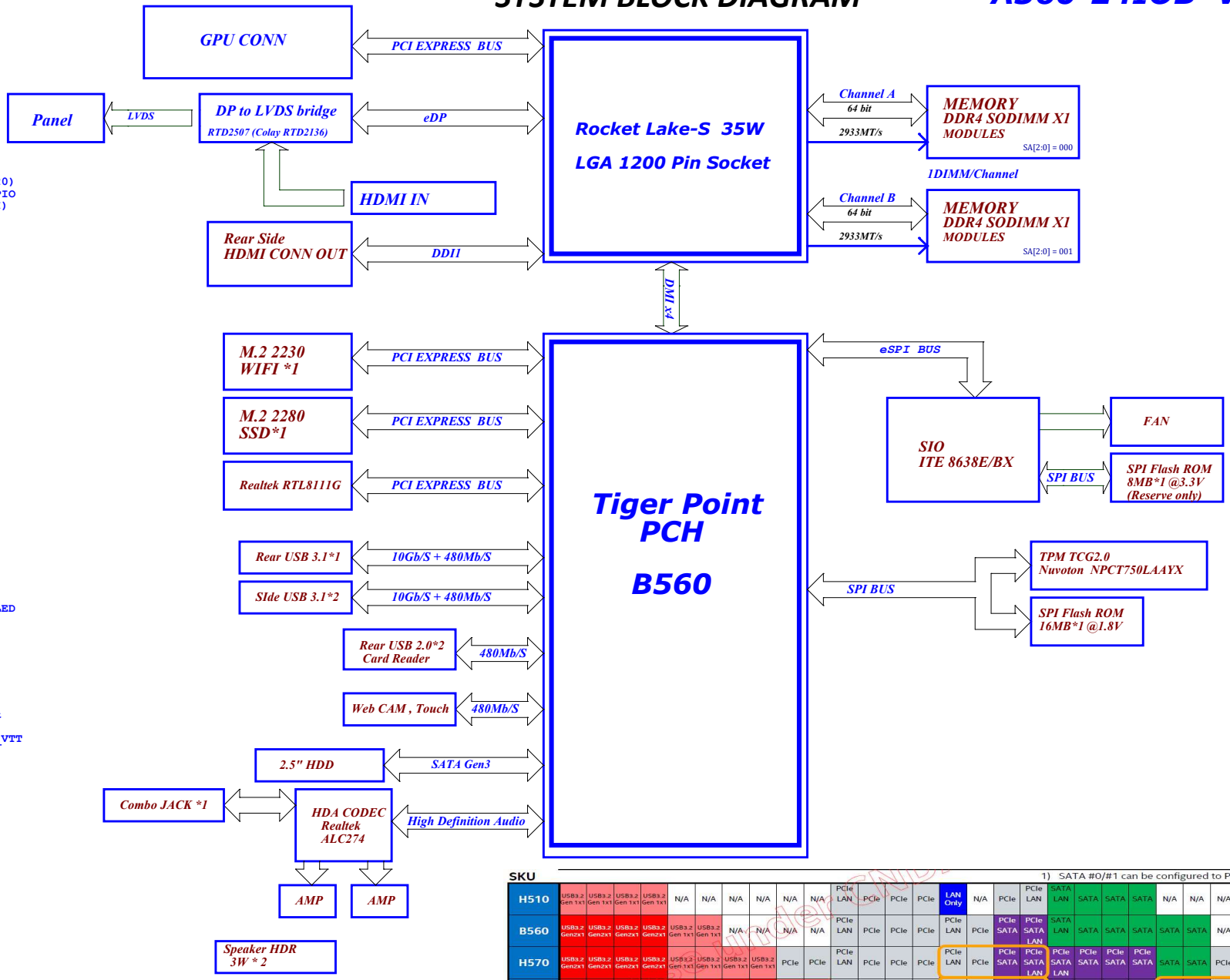


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P59 +20V S5 ADP/INA300
P60 +5V S5/+3V3_S5
P61 +12V_S0/+5V7/+3V3_S0
P62 VCORE CONTROLLER
P63 VCCIA Phase1-4 Output
P64 VCCGT 2 Phase Output
P65 +1V2_DDR4_S3/+0V6_DDR4_VTT
P66 +2V5_VPP_DDR4_S3
P67 +VCCIO_0
P68 +VCCIO_1_2
P69 +VCCIN_AUX
P70 +VCCSA
P71 +VCCST_VCCPLL_S3
P72 12V WiTeless
P73 +1V05_S3
P74 +1V8_S5
P75 GPU PCIe
P76 BLEED OFF
P77-Reserve
P78-Reserve
P79-Reserve
P80-Reserve
P81-Reserve
P82-Reserve
P83-Reserve
P84-Reserve
P86-Reserve
P87-Reserve
P88-Reserve
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P90-Reserve
P91-Reserve
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P93-Reserve
P94-Reserve
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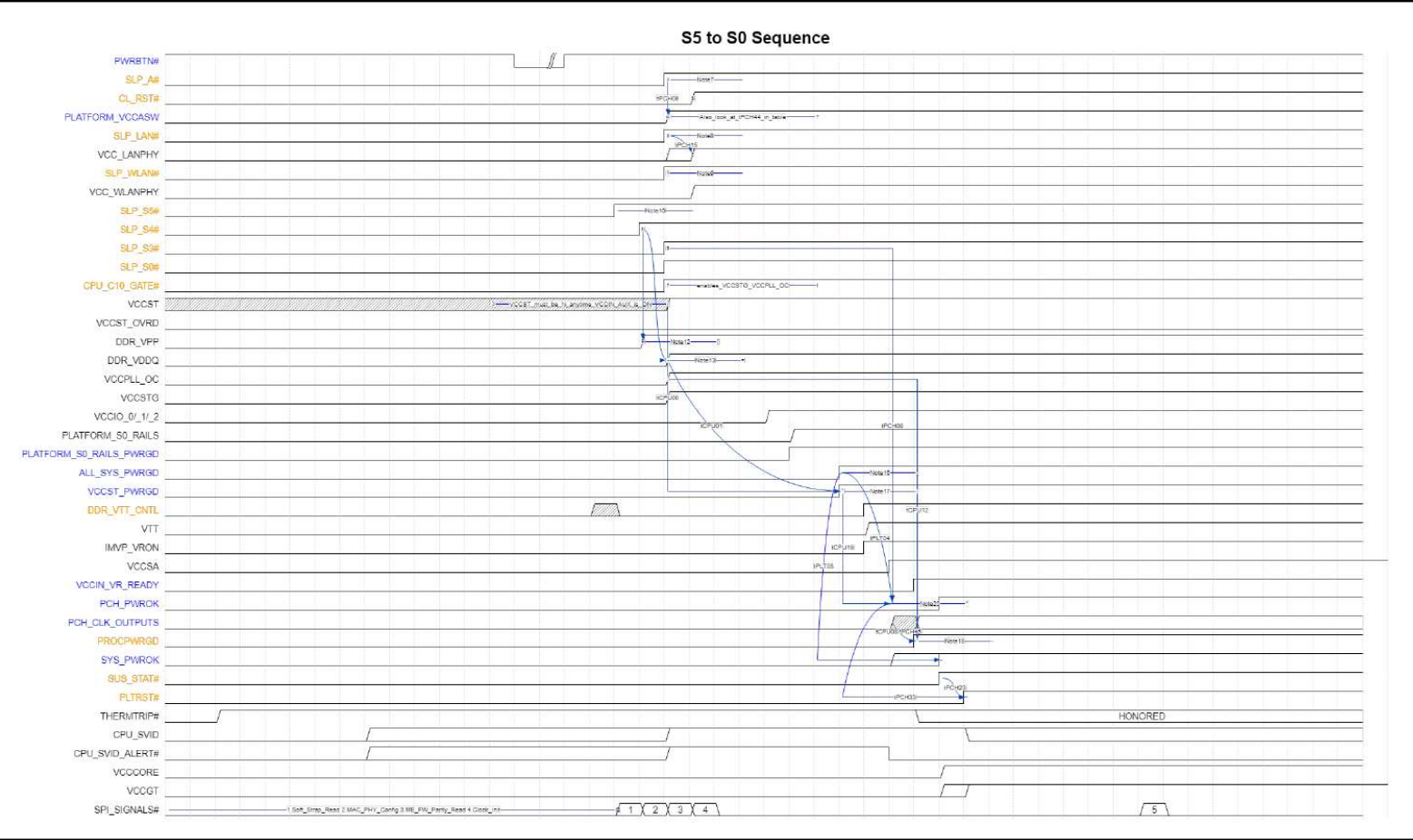
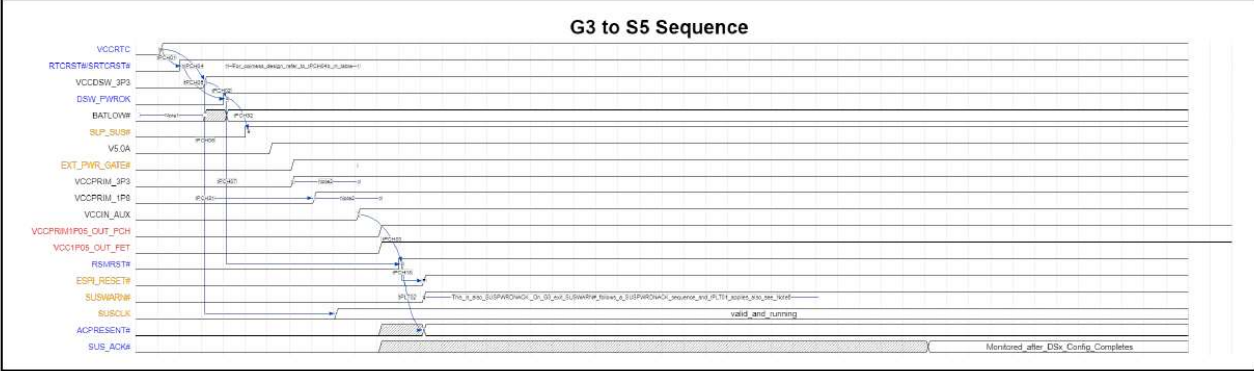
SYSTEM BLOCK DIAGRAM

A560-24IOB Ver. X03




SKU															1) SATA #0/#1 can be configured to PCIe* Ports 11/12 or 13/14.												
H510	USB3.2 Gen1x1	USB3.2 Gen1x1	USB3.2 Gen1x1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	LAN	PCIe	PCIe	PCIe	LAN Only	N/A	PCIe	LAN	SATA	SATA	SATA	SATA	N/A	N/A	N/A	N/A	N/A
B560	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen1x1	USB3.2 Gen1x1	N/A	N/A	N/A	N/A	N/A	LAN	PCIe	PCIe	PCIe	LAN	PCIe	PCIe	SATA	SATA	SATA	SATA	SATA	SATA	N/A	N/A	PCIe	PCIe
H570	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen1x1	USB3.2 Gen1x1	USB3.2 Gen1x1	USB3.2 Gen1x1	USB3.2 Gen1x1	USB3.2 Gen1x1	USB3.2 Gen1x1	LAN	PCIe	PCIe	PCIe	LAN	PCIe	PCIe	SATA	SATA	SATA	SATA	SATA	SATA	PCIe	PCIe	PCIe	PCIe
Q570	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	LAN	PCIe	PCIe	PCIe	LAN	PCIe	PCIe	SATA	SATA	SATA	SATA	SATA	SATA	PCIe	PCIe	PCIe	PCIe
Z590	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	LAN	PCIe	PCIe	PCIe	LAN	PCIe	PCIe	SATA	SATA	SATA	SATA	SATA	SATA	PCIe	PCIe	PCIe	PCIe
W580	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	LAN	PCIe	PCIe	PCIe	LAN	PCIe	PCIe	SATA	SATA	SATA	SATA	SATA	SATA	PCIe	PCIe	PCIe	PCIe

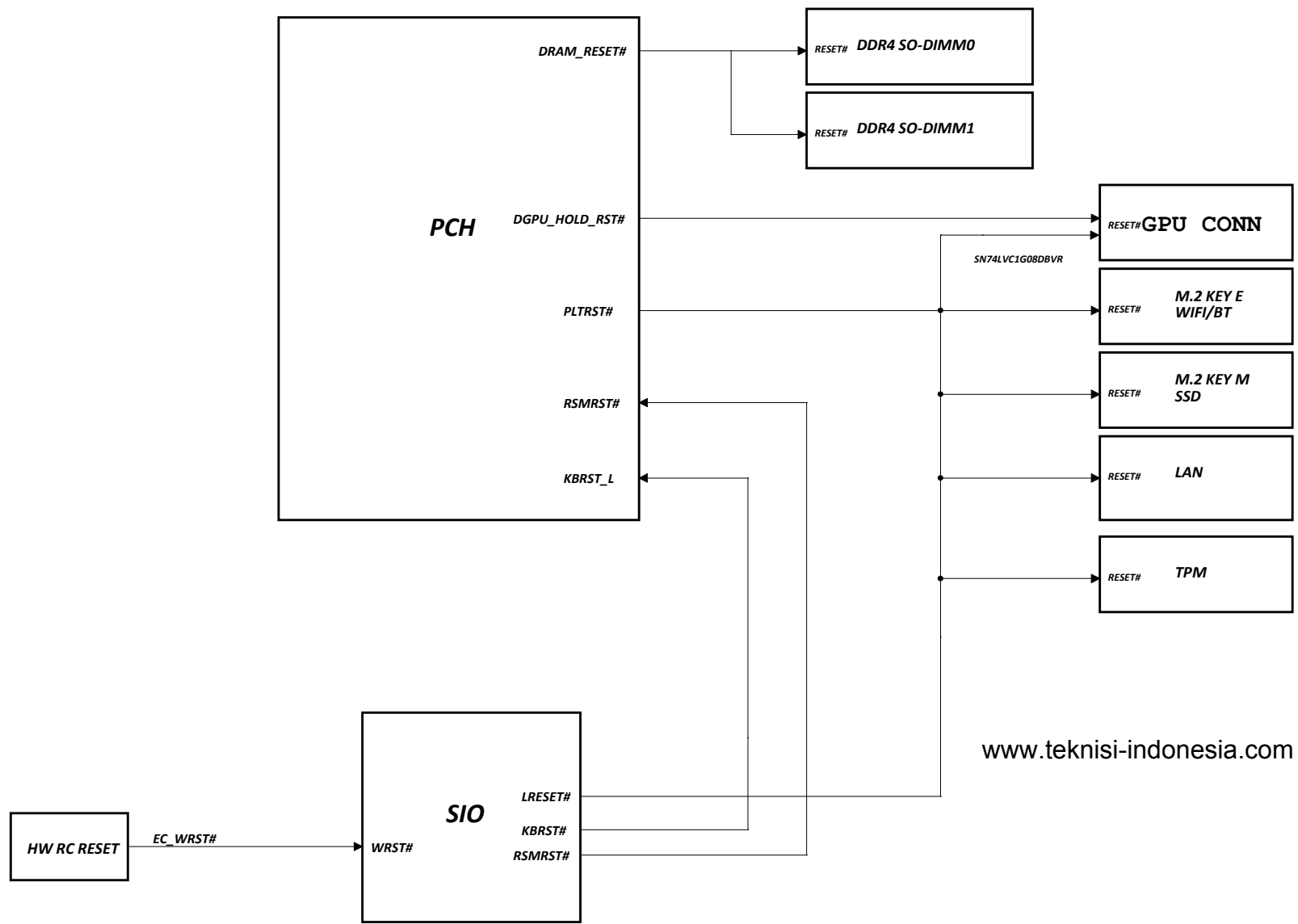
Timing Diagram for G3 to S0 [Deep Sx Platform]





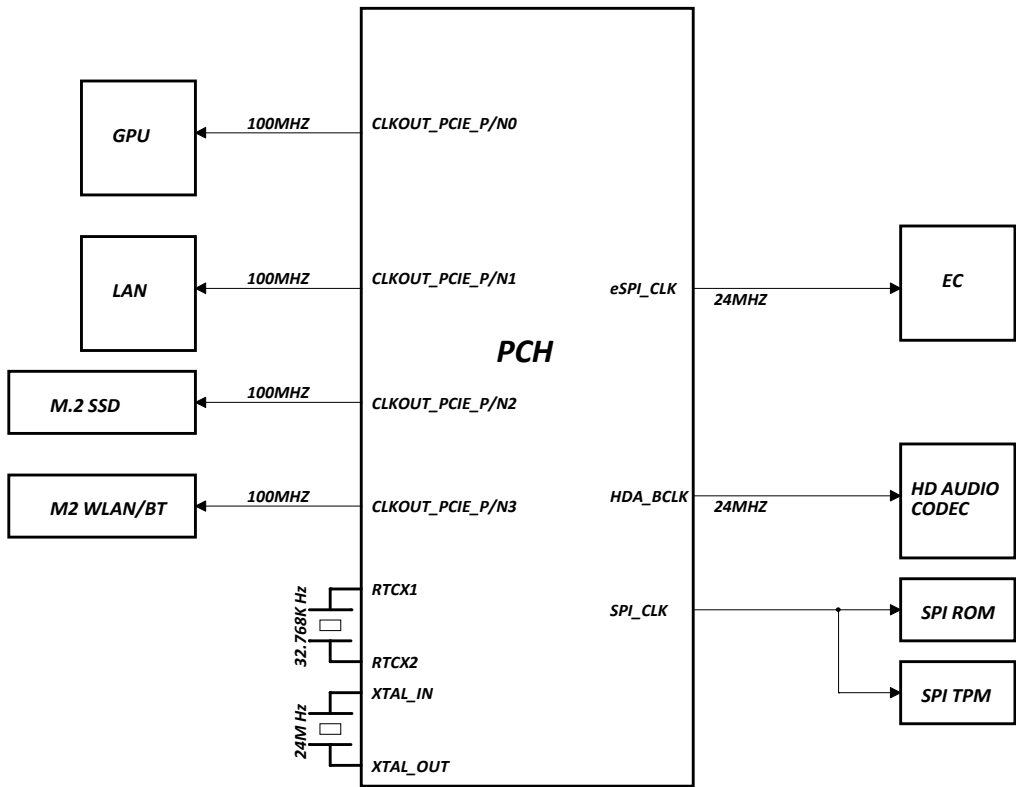
 Asia Vital Components Co., Ltd.			
TitlePOWER MAP			
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RST MAP

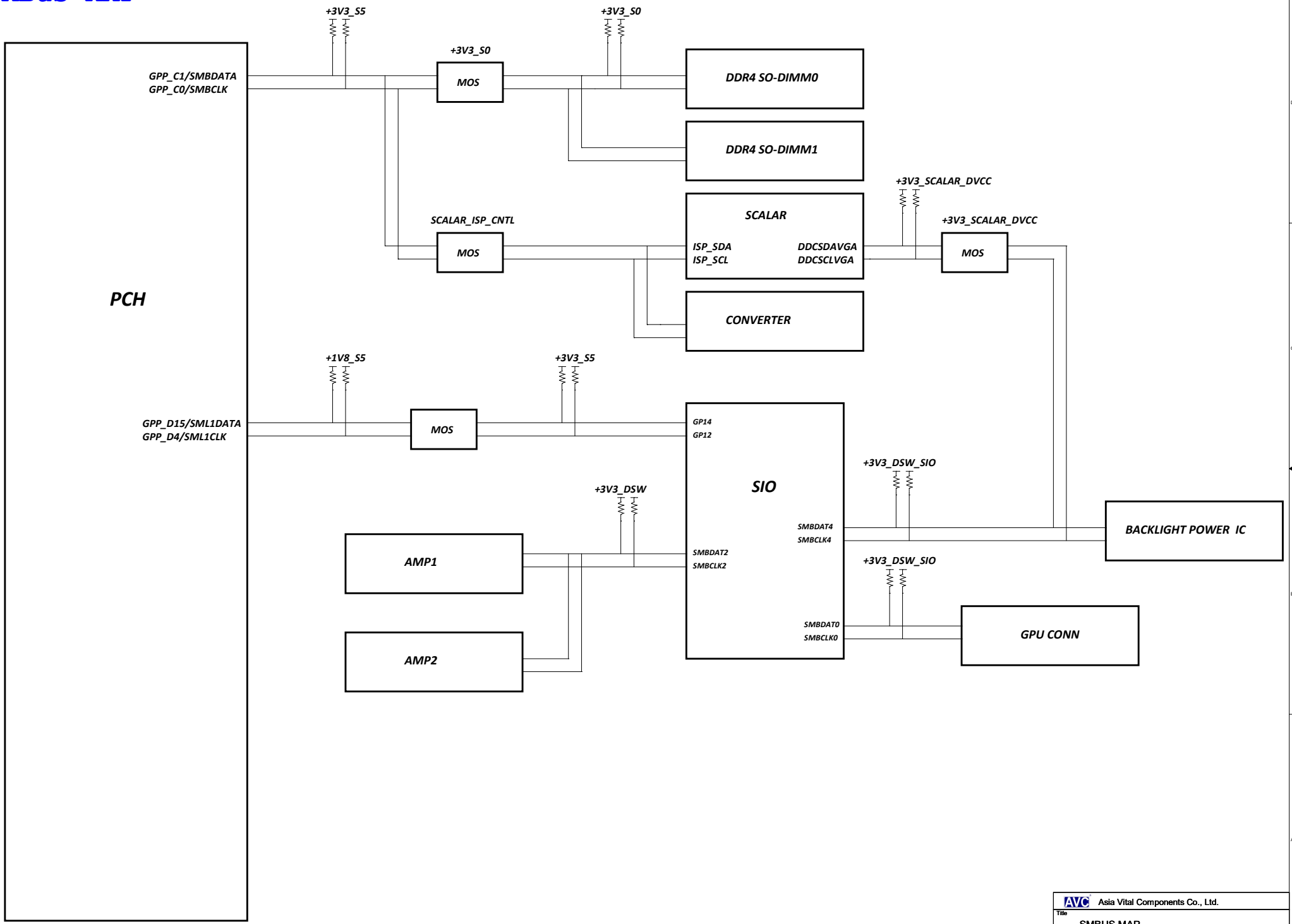


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CLOCKS DIAGRAM



SMBus MAP



HW STRAPING

Table 22. Pin Straps


Signal	Usage	When Sampled	Comment
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The strap has a 20 kOhm ± 30% internal pull-down. 0=>Disable "Top Swap" mode. (Default) 1=>Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A[23:16]) as selected in Top Swap Block size soft strap. . <i>Notes:</i> 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCH, bit4). 4. This signal is in the primary well.
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The strap has a 20 kOhm ± 30% internal pull-down. 0=>Disable "No Reboot" mode. (Default) 1=>Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/ XDP. <i>Notes:</i> 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0=>Disable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1=>Enable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel® AKT with TLS. <i>Notes:</i> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_C5 / SMI0ALERT#	eSPI Disable	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0 = Enable eSPI. (Default)
continued...			

Signal	Usage	When Sampled	Comment
			1 = Disable eSPI. <i>Notes:</i> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 4.7 kOhm pull up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_G9 / ISH_SPI_CLK / DDP3_CTRLDATA / GSPI2_CLK / TBT_L5X2_RXD	DDP3 I2C / TBT_L5X2 / BBSB_L52 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0 = DDP3 I2C / TBT_L5X2 / BBSB_L52 pins at 1.8V 1 = DDP3 I2C / TBT_L5X2 / BBSB_L52_TX pins at 3.3V <i>Notes:</i> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_G11 / ISH_SPI_MOSI / DDP4_CTRLDATA / GSPI2_MOSI / TBT_L5X3_RXD	DDP4 I2C / TBT_L5X3 / BBSB_L53 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0 = DDP4 I2C / TBT_L5X3 / BBSB_L53 pins at 1.8V 1 = DDP4 I2C / TBT_L5X3 / BBSB_L53 pins at 3.3V <i>Notes:</i> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_B23 / SMI1ALERT# / PCHHOT#	CPUNSSC Clock Frequency	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0 = 38.4 MHz clock (direct from crystal) (default) 1 = 19.2 MHz clock (derived from 38.4 MHz crystal) <i>Notes:</i> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. 3. This signal is in the primary well.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100 K if pulled up to 3.3 V or 75 K if pulled up to 1.8 V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100 K if pulled up to 3.3 V or 75 K if pulled up to 1.8 V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_R2 / HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This strap has a 20 kOhm ± 30% internal pull-down. 0=> Enable security measures defined in the Flash Descriptor. (Default) 1=> Disable Flash Descriptor Security (<u>override</u>). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. <i>Notes:</i> 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H12 / SMI2ALERT#	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0=>Master Attached Flash Sharing (MAFS) enabled (Default) 1=>Slave Attached Flash Sharing (SAFS) enabled. <i>Notes:</i> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
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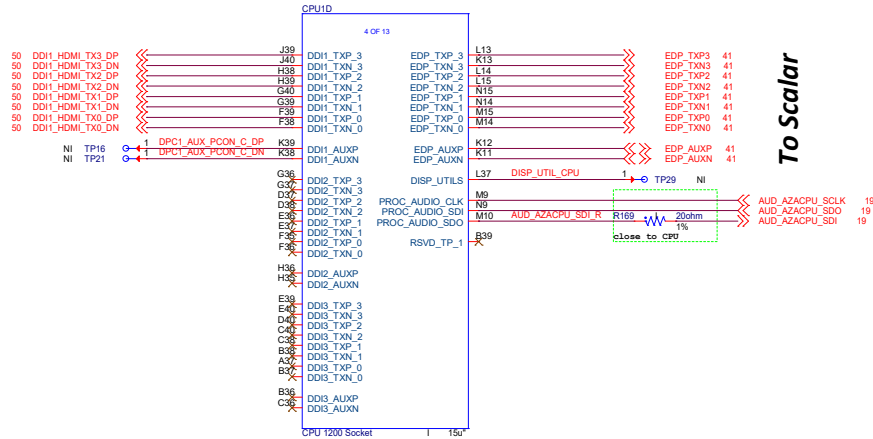
Signal	Usage	When Sampled	Comment
GPP_H15 / SMI3ALERT#	Reserved	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0=> JTAG ODT is disabled 1=> JTAG ODT is enabled <i>Notes:</i> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_H18 / SMI4ALERT#	VCCSPI Voltage Configuration	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0=> VCCSPI at 3.3 V (Default) 1=> VCCSPI at 1.8 V <i>Notes:</i> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_G13 / DDP1_CTRLDATA / TBT_L5X0_RXD	DDP1 I2C / TBT_L5X0 / BBSB_L50 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0=> DDP1 I2C / TBT_L5X0 / BBSB_L50 pins at 1.8V 1=> DDP1 I2C / TBT_L5X0 / BBSB_L50 pins at 3.3V <i>Notes:</i> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_G15 / DDP2_CTRLDATA / TBT_L5X1_RXD	DDP2 I2C / TBT_L5X1 / BBSB_L501 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0=> = DDP2 I2C / TBT_L5X1 / BBSB_L51 pins at 1.8V 1=> = DDP2 I2C / TBT_L5X1 / BBSB_L51 pins at 3.3V <i>Notes:</i> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
DBG_PMODE	Reserved	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-up. This strap should sample high. There should NOT be any on-board device driving it to opposite direction during strap sampling. <i>Notes:</i> 1. The internal pull-up is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPD7	Reserved	Rising edge of DSW_PWROK	This strap has a 20 kOhm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. <i>Notes:</i> 1. The internal pull-down is disabled after DSW_PWROK is high. 2. This signal is in the DSW well.
GPP_J2 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Selection	Rising edge of RSMRST#	This strap has a 20 kOhm ± 30% internal pull-down. 0 = 38.4 MHz (default) 1 = 24 MHz <i>Notes:</i> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J4 / CNV_RGI_DT / UART0_TXD	M.2 CNVi Mode Select	Rising edge of RSMRST#	This strap does not have an internal pull-up or pull-down. A weak external pull-up is required. 0=>Integrated CNVi enabled. 1=>Integrated CNVi disabled. <i>Note:</i> When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down resistor will pull the strap low to enable CNVi interface.
GPP_B22 / GSPI1_MOSI	Boot BIOS Strap (BBS)	Rising edge of PCH_PWROK	This signal has a 20 kOhm ± 30% internal pull-down.

Signal	Usage	When Sampled	Comment
			0=>BIOS fetches are routed to SPI (MAF) or the eSPI Flash Channel (SAF) 1=>BIOS fetches are routed to the eSPI Peripheral Channel 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.

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HDMI OUT



To Scalar

DGPU

DMI X4

RX

Intel® 500 Series Chipset SKU Plan - Preliminary (cont.)

Feature / Capability	W580	Q570	Z590	H570	B560	H510
IA & BLCK Overclocking						
Memory Overclocking	✓		✓			
Processor						
Processor PCI Express 4.0 Lanes Configuration Support	1x16+1x4 or 2x8 + 1x4 or 1x8+3x4	1x16+1x4 or 2x8 + 1x4 or 1x8+3x4	1x16+1x4 or 2x8 + 1x4 or 1x8+3x4	1x16+1x4	1x16	1x16
Number of Simultaneous Independent Displays Supported	3	3	3	3	3	2
DMI 3.0 Lanes ³	8	8	8	8	4	4
System Memory Channels/DPC	2/2	2/2	2/2	2/2	2/2	2/1
Intel® Stable Image Platform		✓	✓	✓	✓	✓
Storage						
Intel® Optane™ Memory Support	✓	✓	✓	✓	✓	✓
Intel® Rapid Storage Technology 18.5 ¹	✓	✓	✓	✓	✓	✓
• PCIe® Storage Support	✓	✓	✓	✓	✓	✓
• PCIe RAID 0,1,5 Support	✓	✓	✓	✓	✗	✗
• SATA RAID 0,1,5,10 Support	✓	✓	✓	✓	✗	✗
• CPU attached PCIe Storage ⁴	✓	✓	✓	✓	✗	✗

AVC Asia Vital Components Co., Ltd.

Title CPU (PEG, DMI, DDI, EDP)

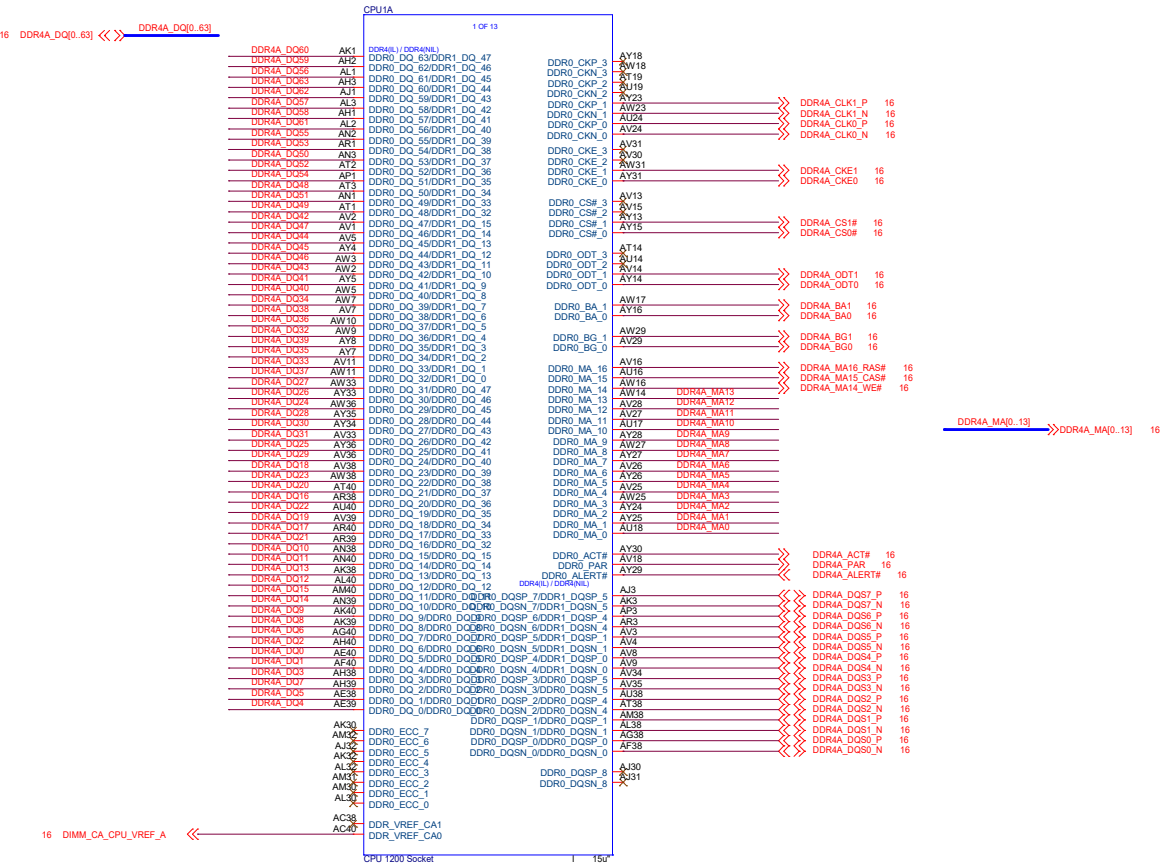
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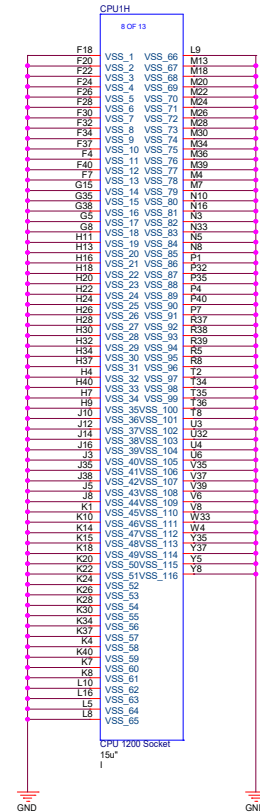
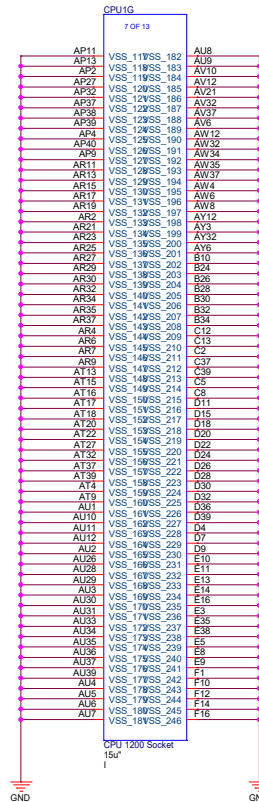
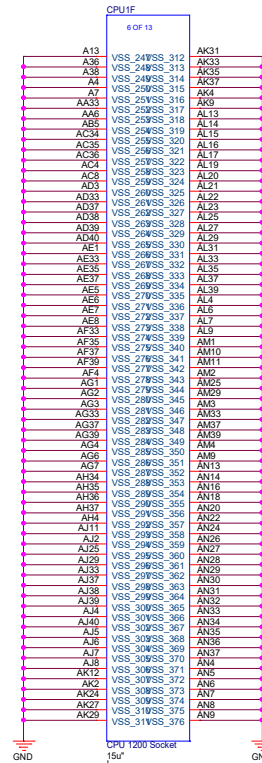
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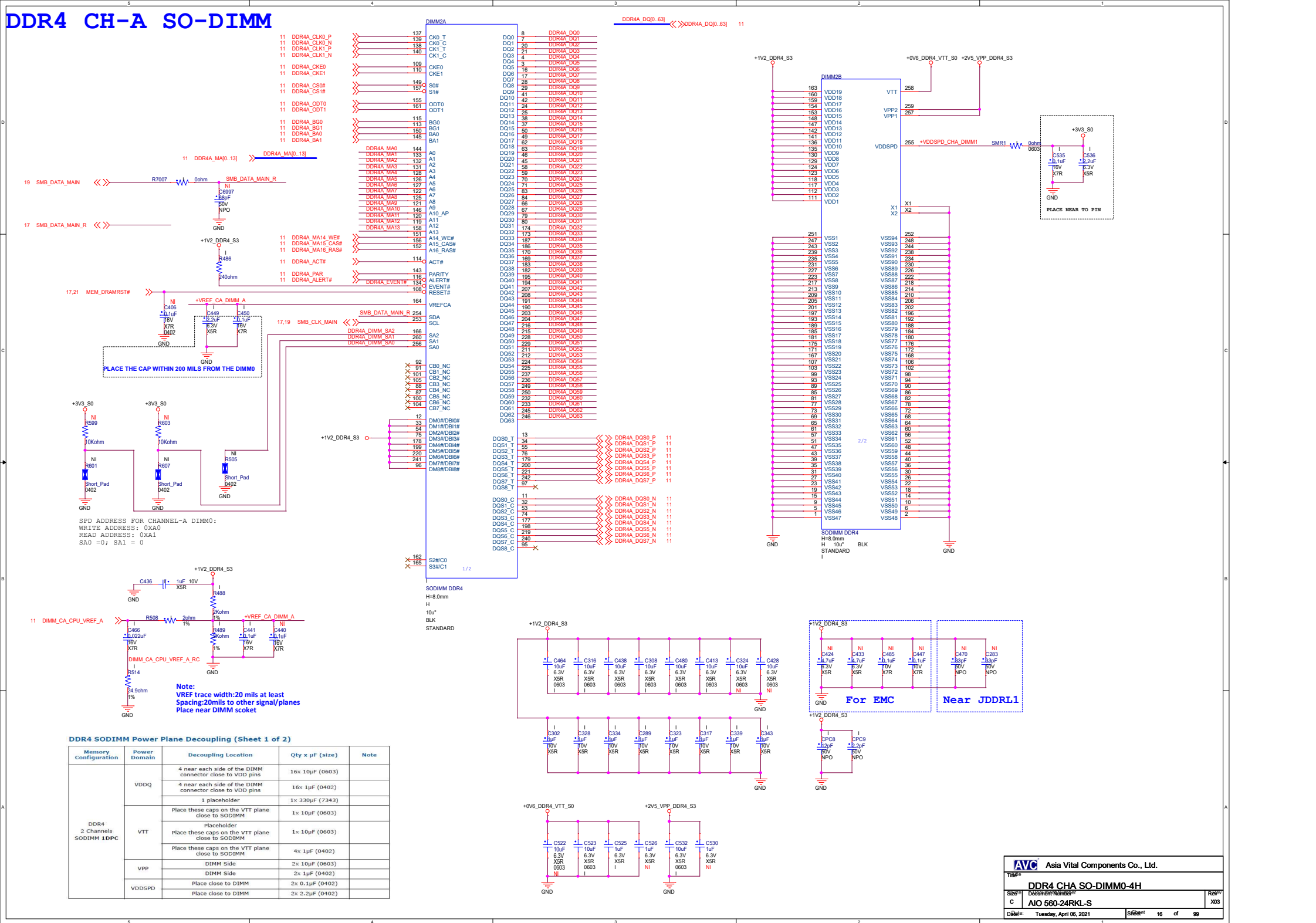
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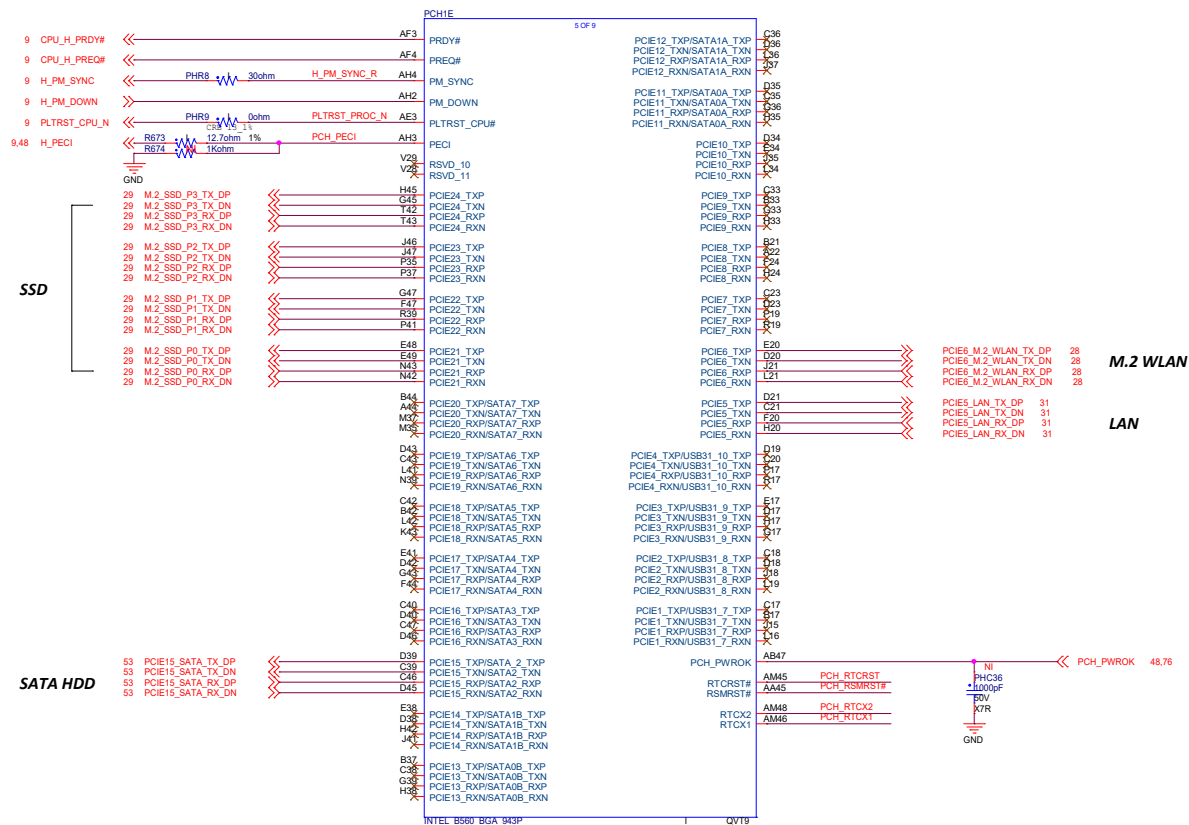
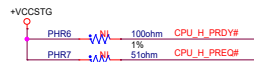




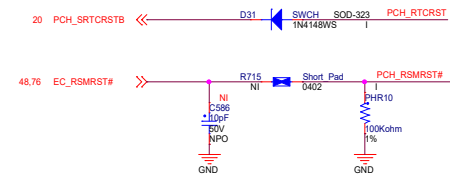
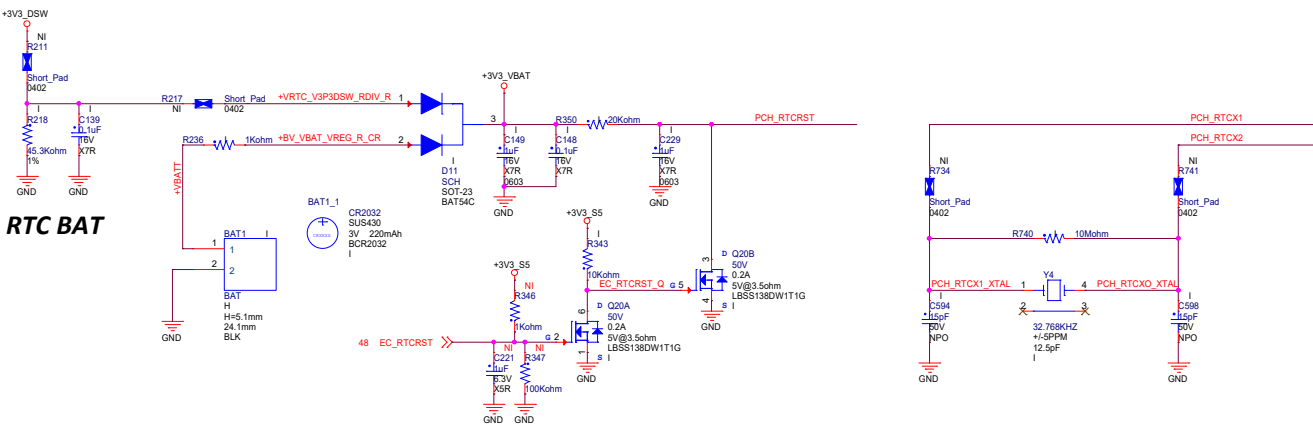


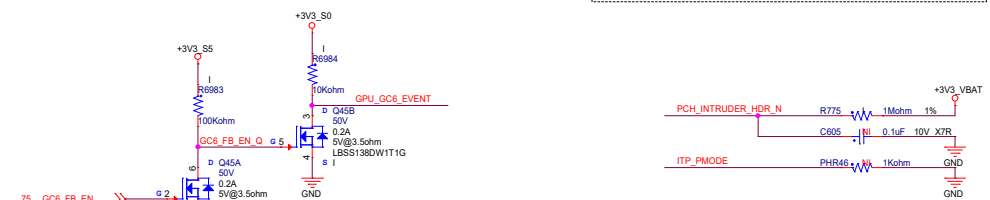
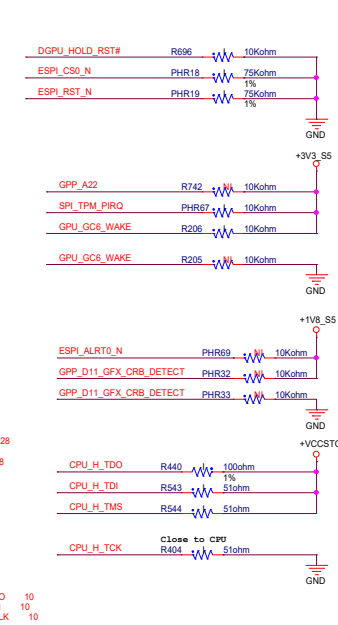
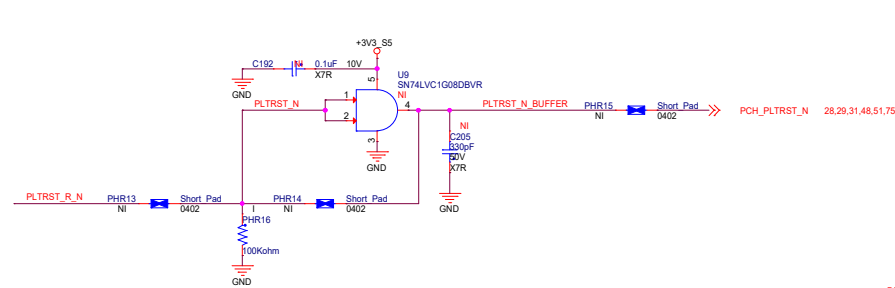
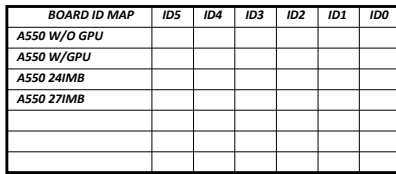
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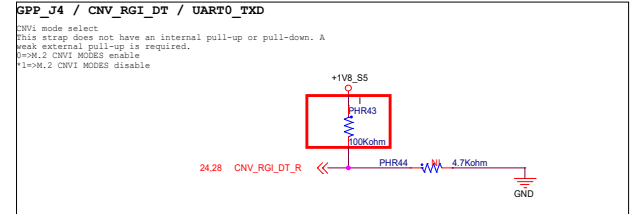
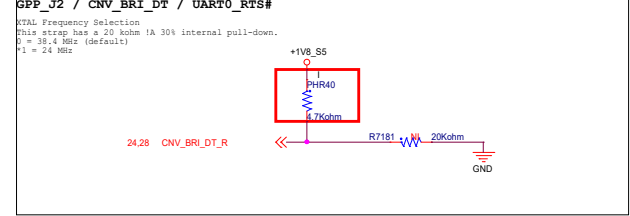
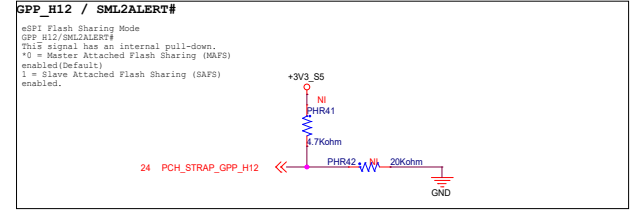
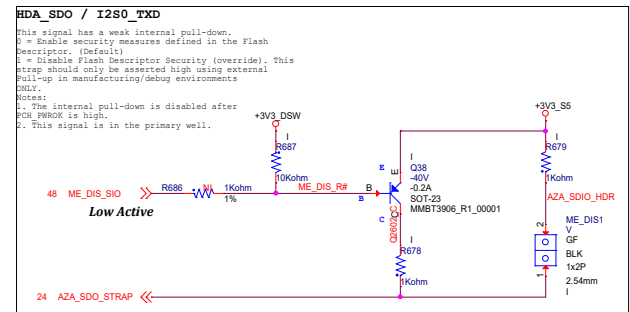
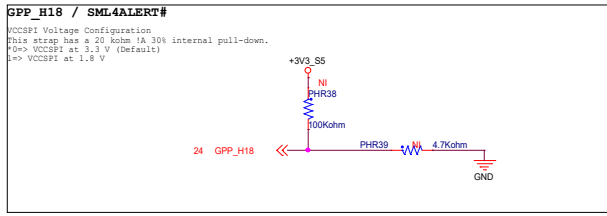
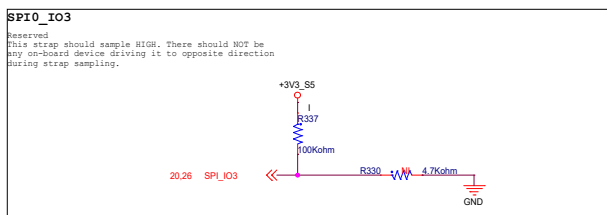
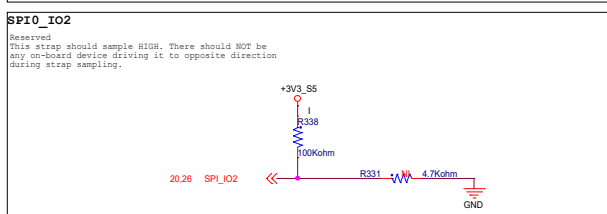
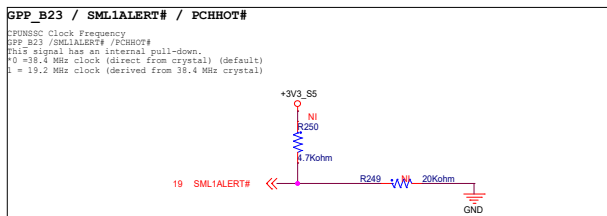
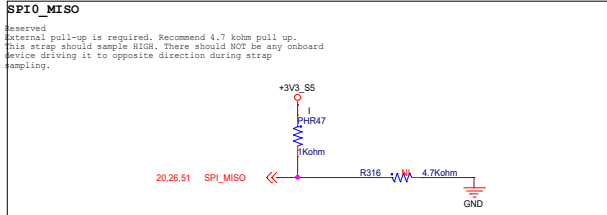
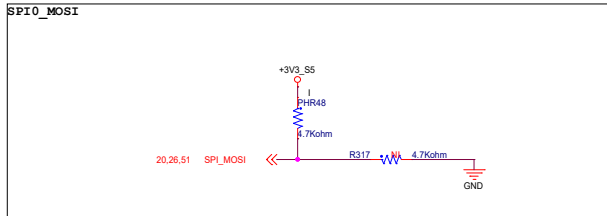
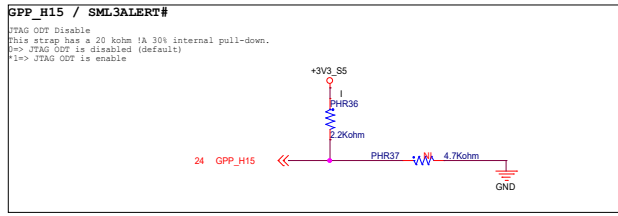
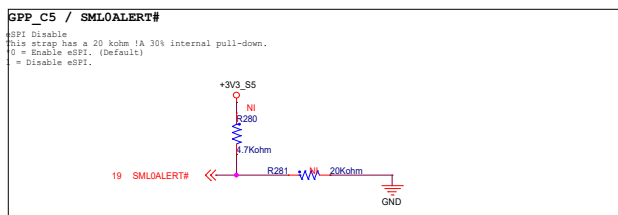
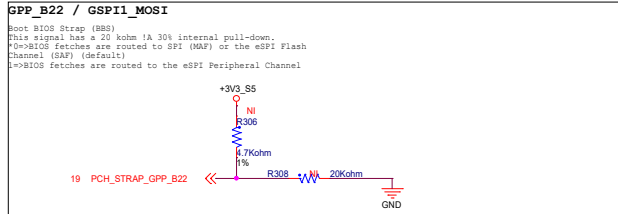
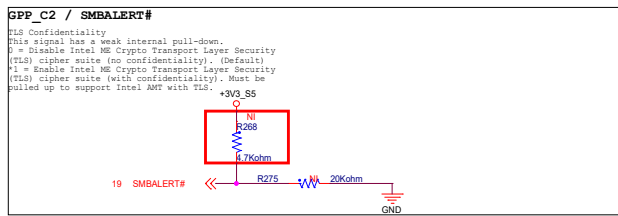
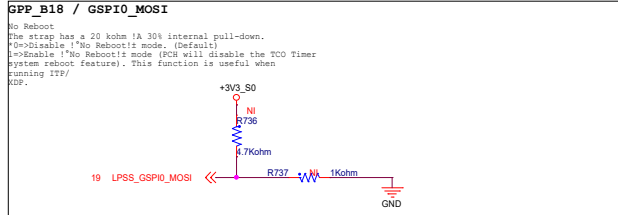
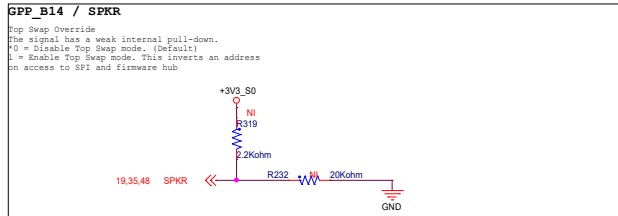


USB2 Port	IO FUNCTION	OC No.
PORT 1	SIDE IO (UP) - P1 : USB3.1 Gen2	OC0
PORT 2	SIDE IO (DN) - P2 : USB3.1 Gen2	OC0
PORT 3		
PORT 4	REAR IO - : USB2.0	OC1
PORT 5	REAR IO - : USB2.0	OC1
PORT 6	REAR IO - P4: USB3.1 Gen2	OC3
PORT 7	TOUCH	
PORT 8	CAMERA	
PORT 9	CARD READER	
PORT 10		
PORT 11		
PORT 12		
PORT 13		
PORT 14	M.2 BT	

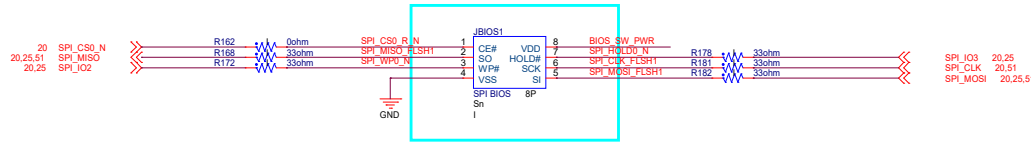




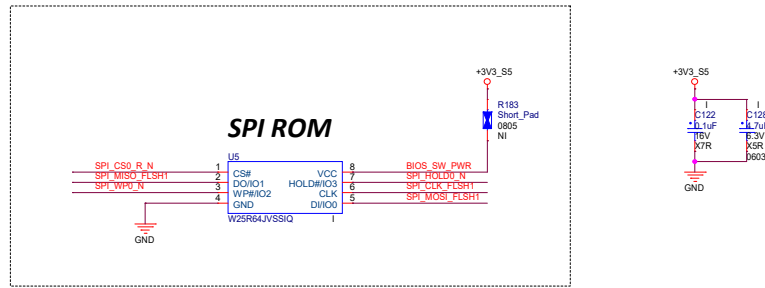
PCH STRAPS



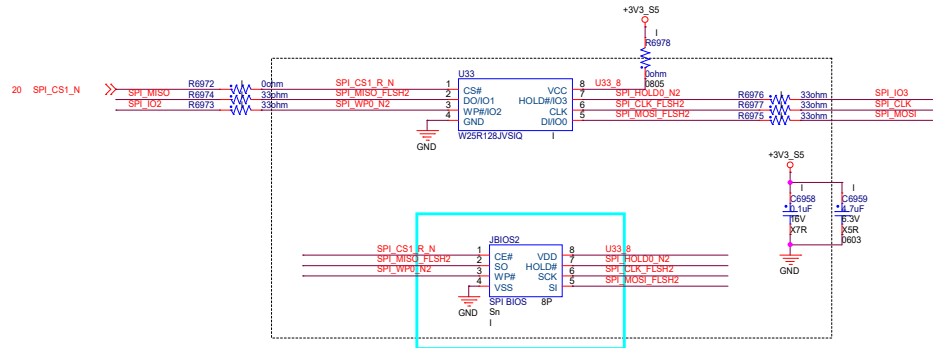
SPI SOCKET



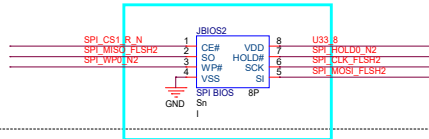
SPI ROM



Co-lay JBIOS1

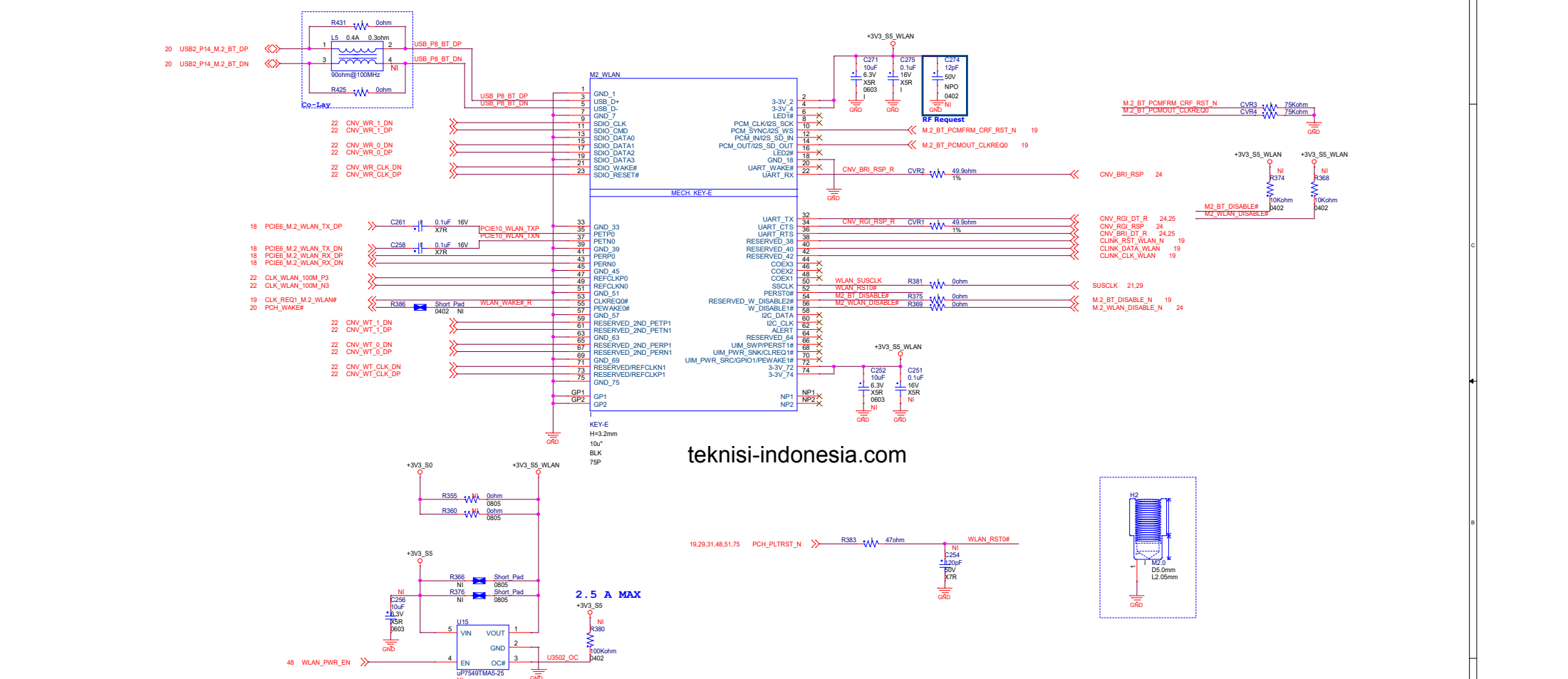


Co-lay JBIOS2

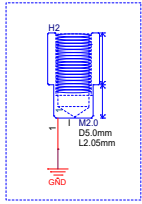


RESERVED

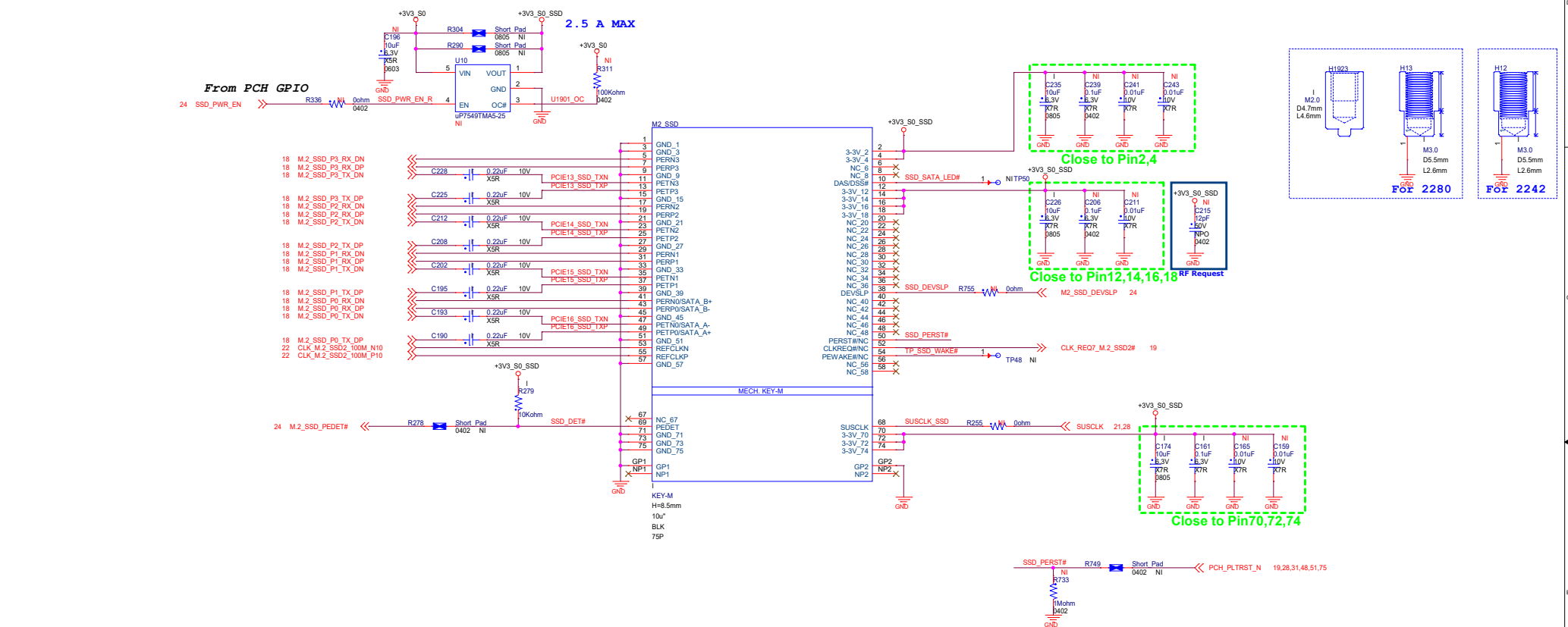
M.2 WLAN 2230 Key-E



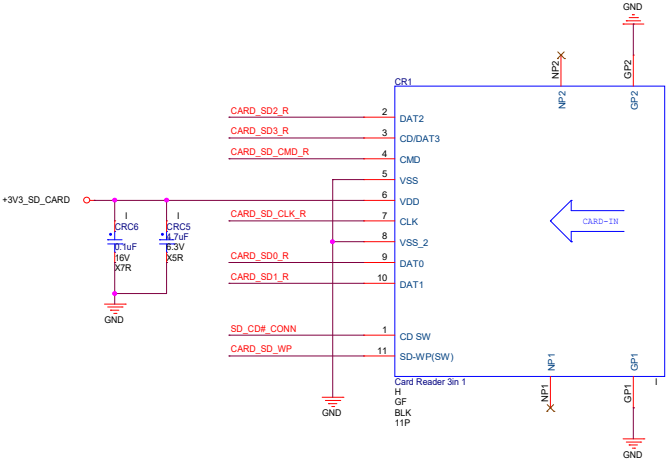
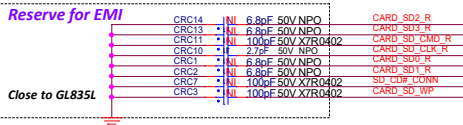
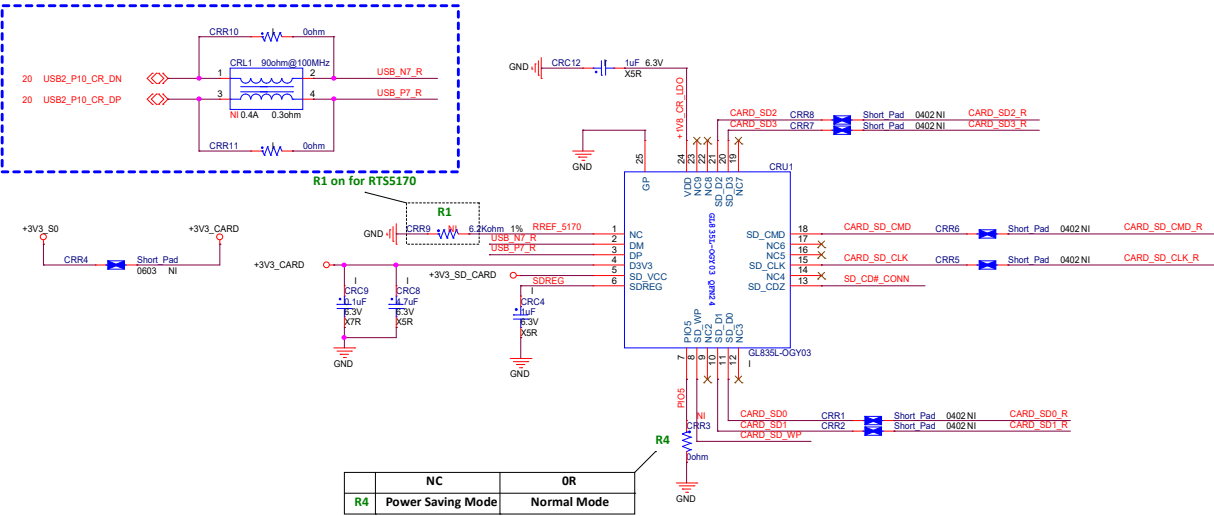
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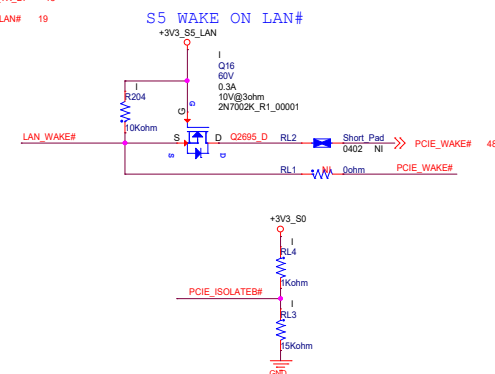
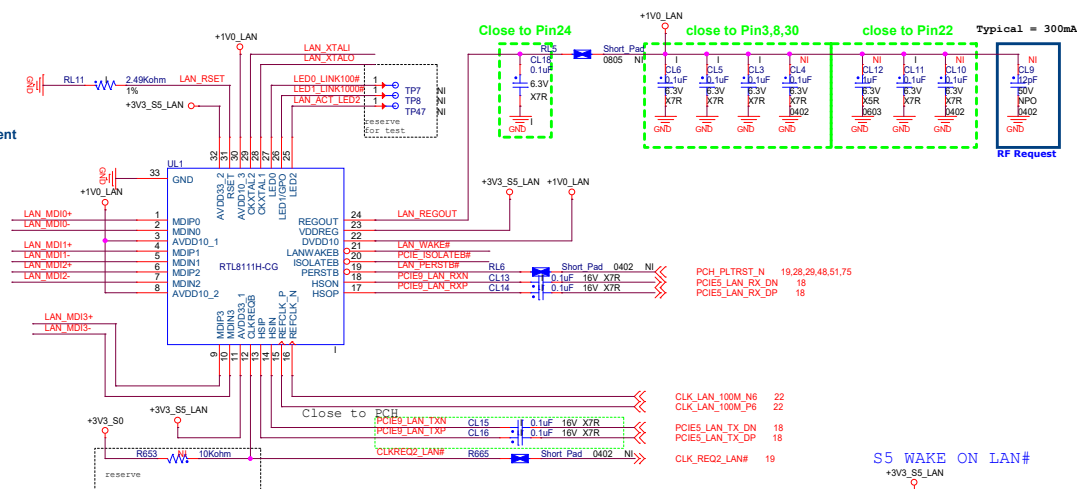
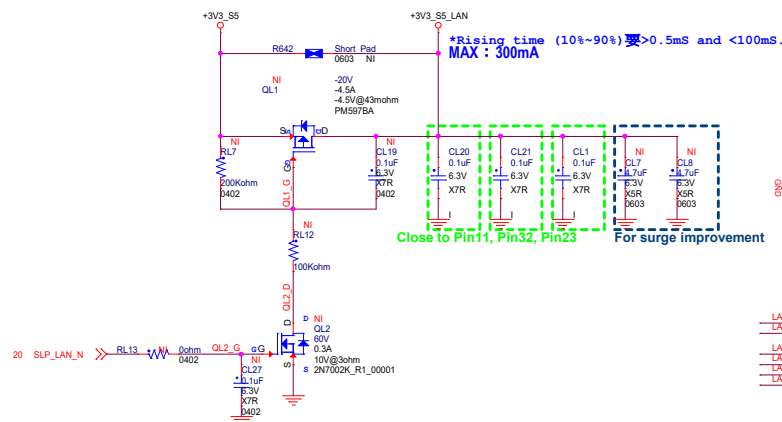
M.2 SSD 2242/ 2280



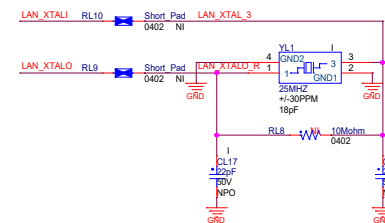
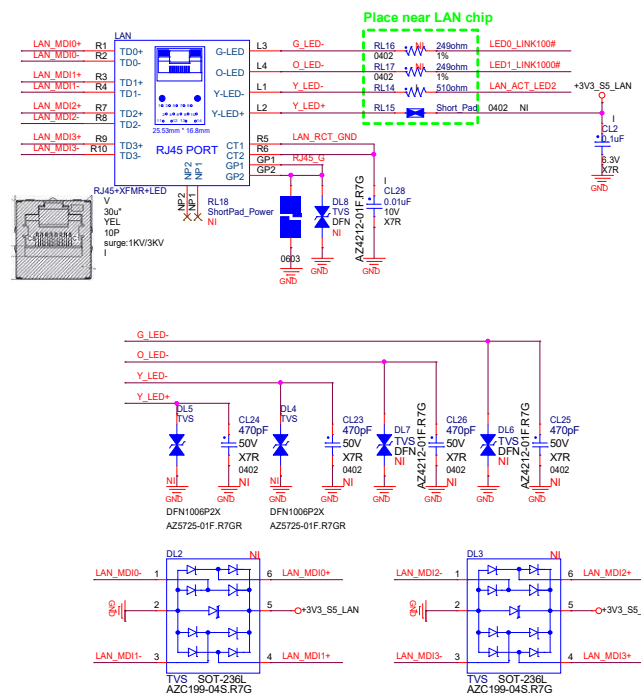
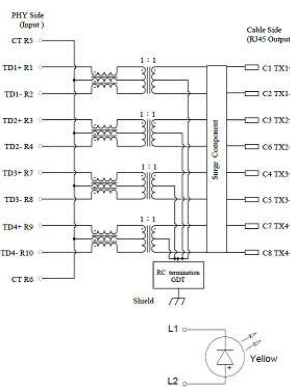
CARD READER GL835L



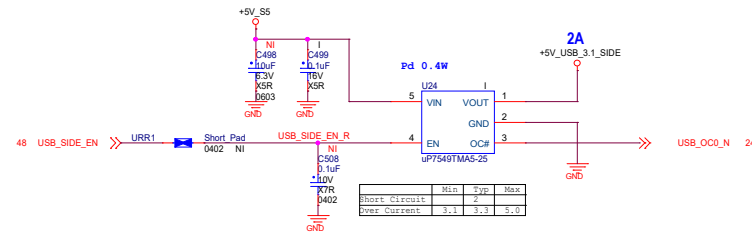
5	4
LAN RTL8111H-CG/ RJ45 CONN	



WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M_inactive	
on	10M_active	
on	100M_inactive	
on	100M_active	
on	1G_inactive	
on	1G_active	



USB3.1_SIDE1

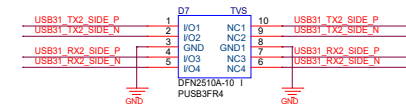
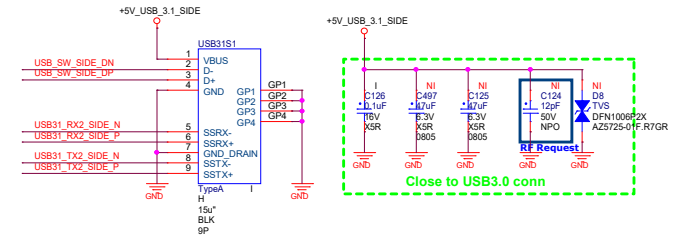
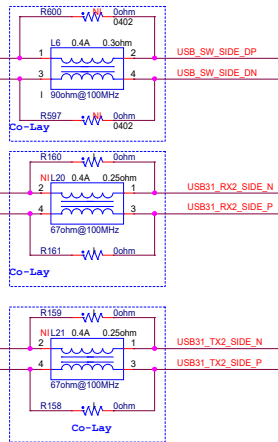


33 USB_SW_SIDE_DN
33 USB_SW_SIDE_DP

20 USB2_P2_SIO_DP
20 USB2_P2_SIO_DN

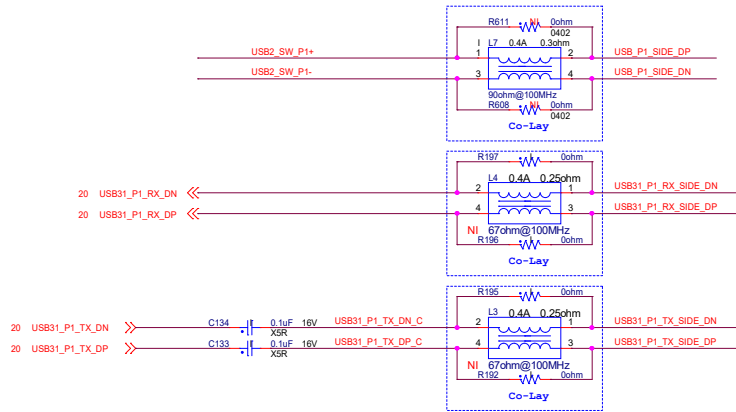
20 USB31_P2_RX_DN
20 USB31_P2_RX_DP

20 USB31_P2_TX_DN
20 USB31_P2_TX_DP

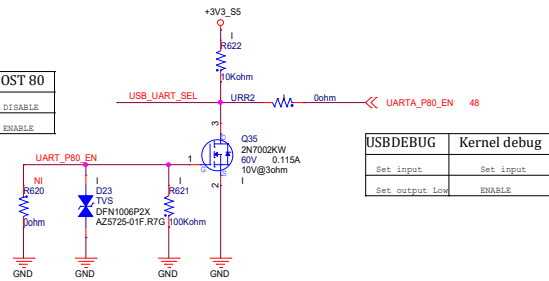


USB3.1_SIDE2

32 USB_SW_SIDE_DN << _____
32 USB_SW_SIDE_DP << _____

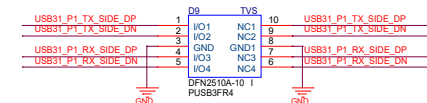
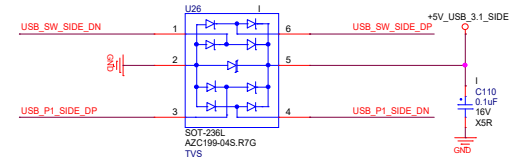
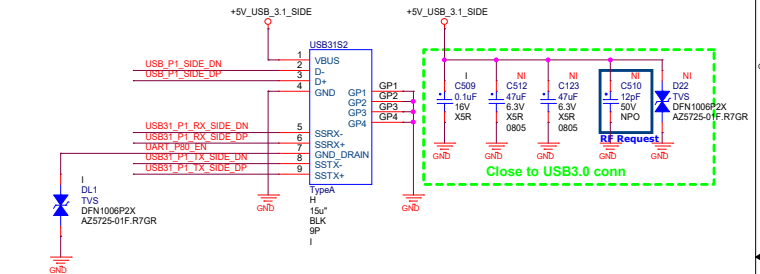
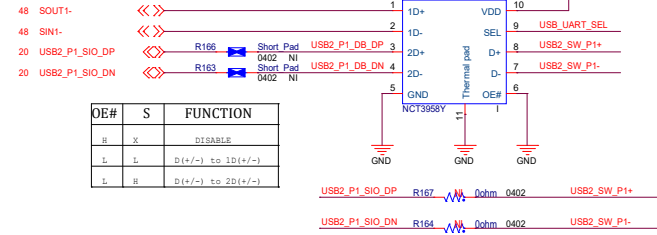


UART_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

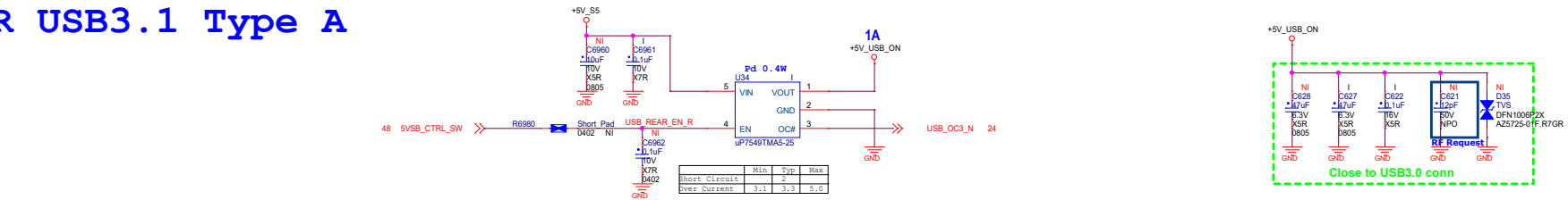


USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

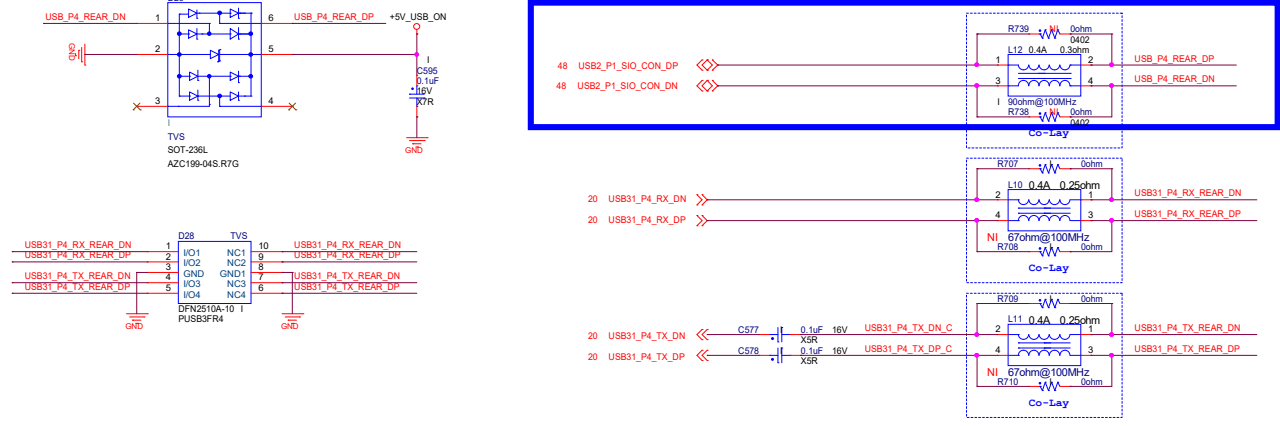
USB Debug Function



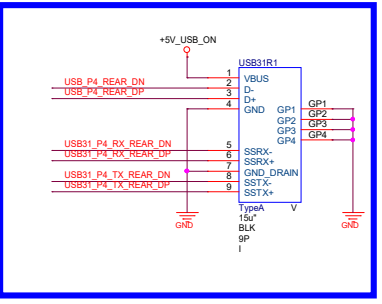
REAR USB3.1 Type A



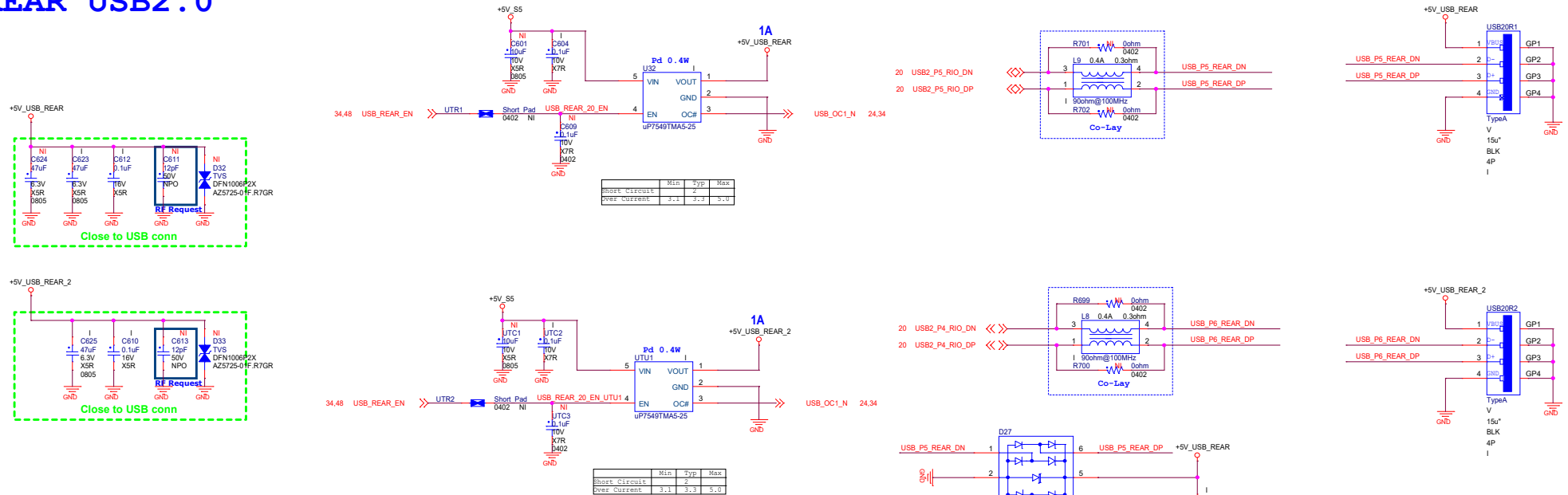
USB Smart Power on



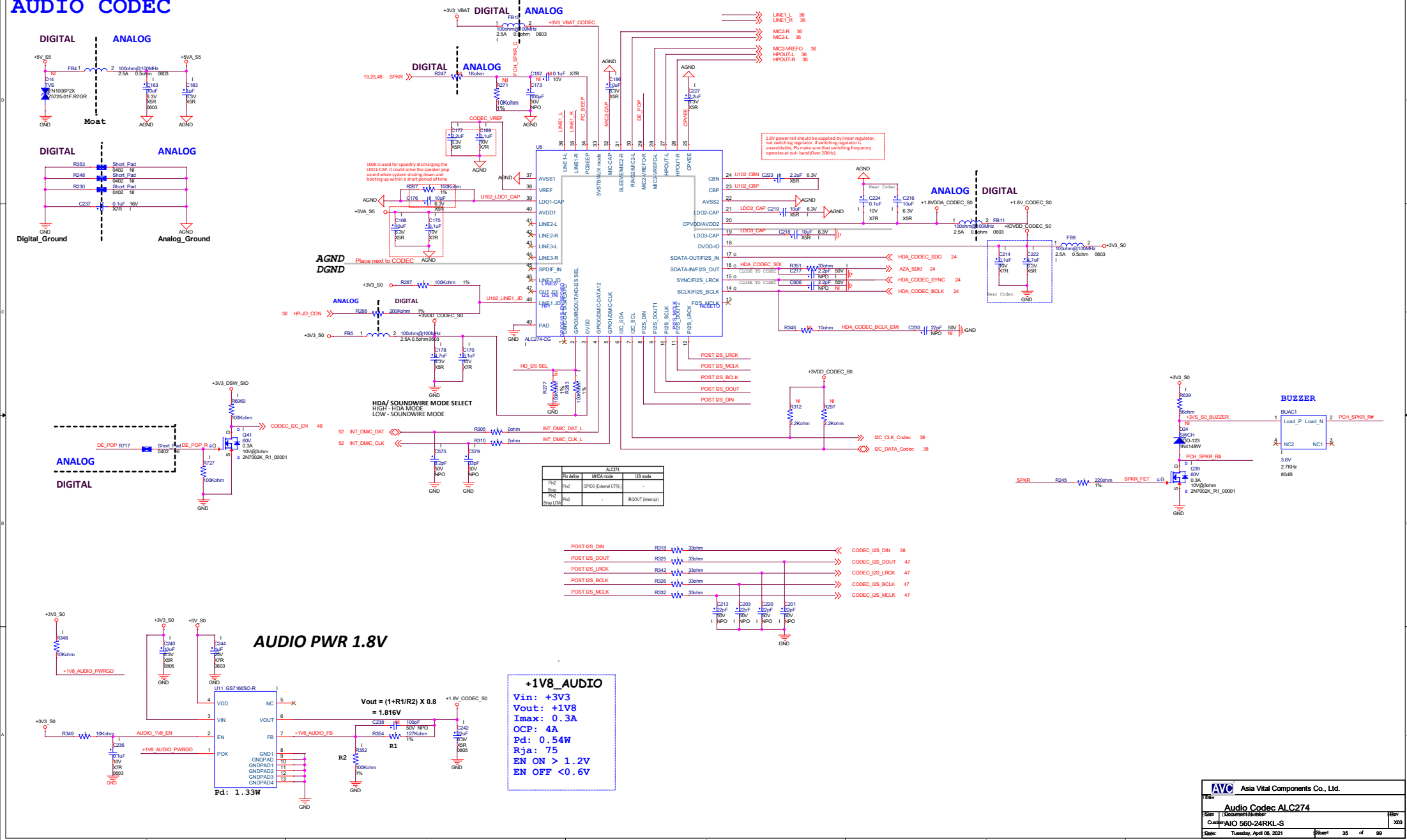
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REAR USB2.0

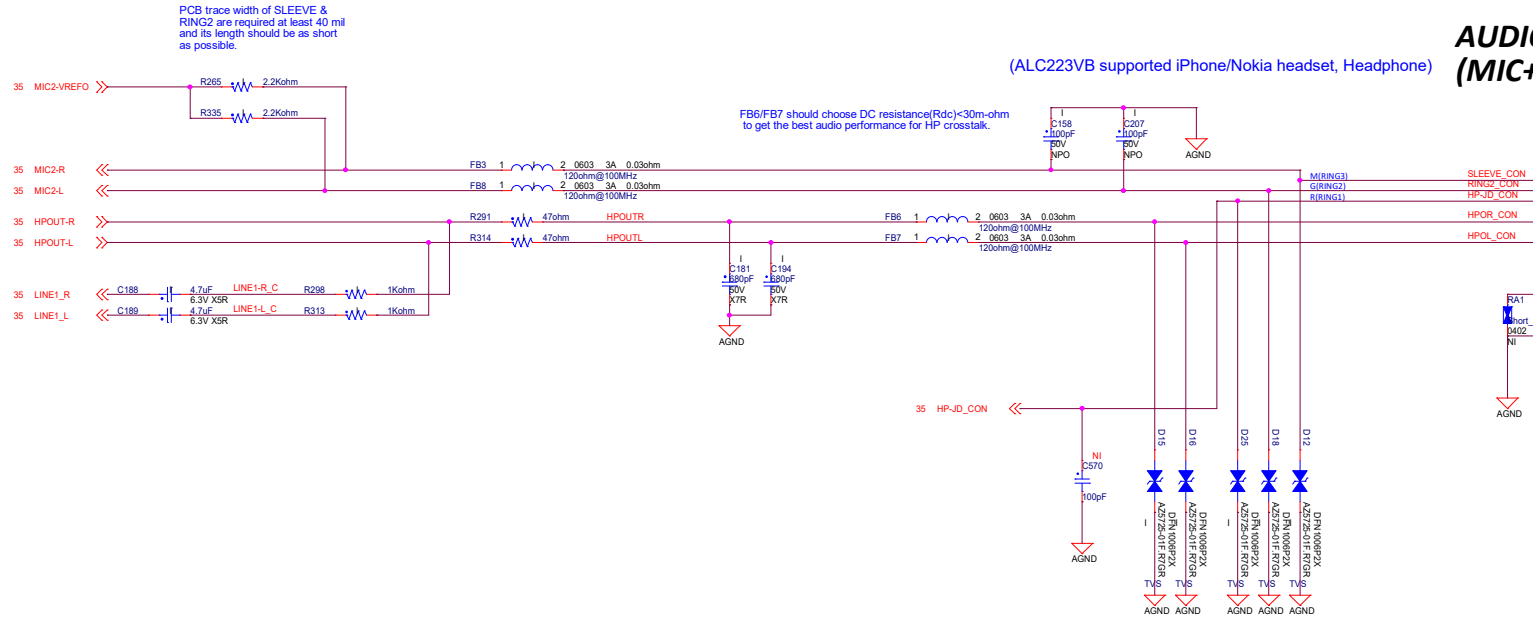


AUDIO CODEC

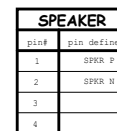


AUDIO COMBO JACK (MIC+HEADPHONE)

(ALC223VB supported iPhone/Nokia headset, Headphone)

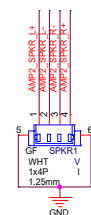
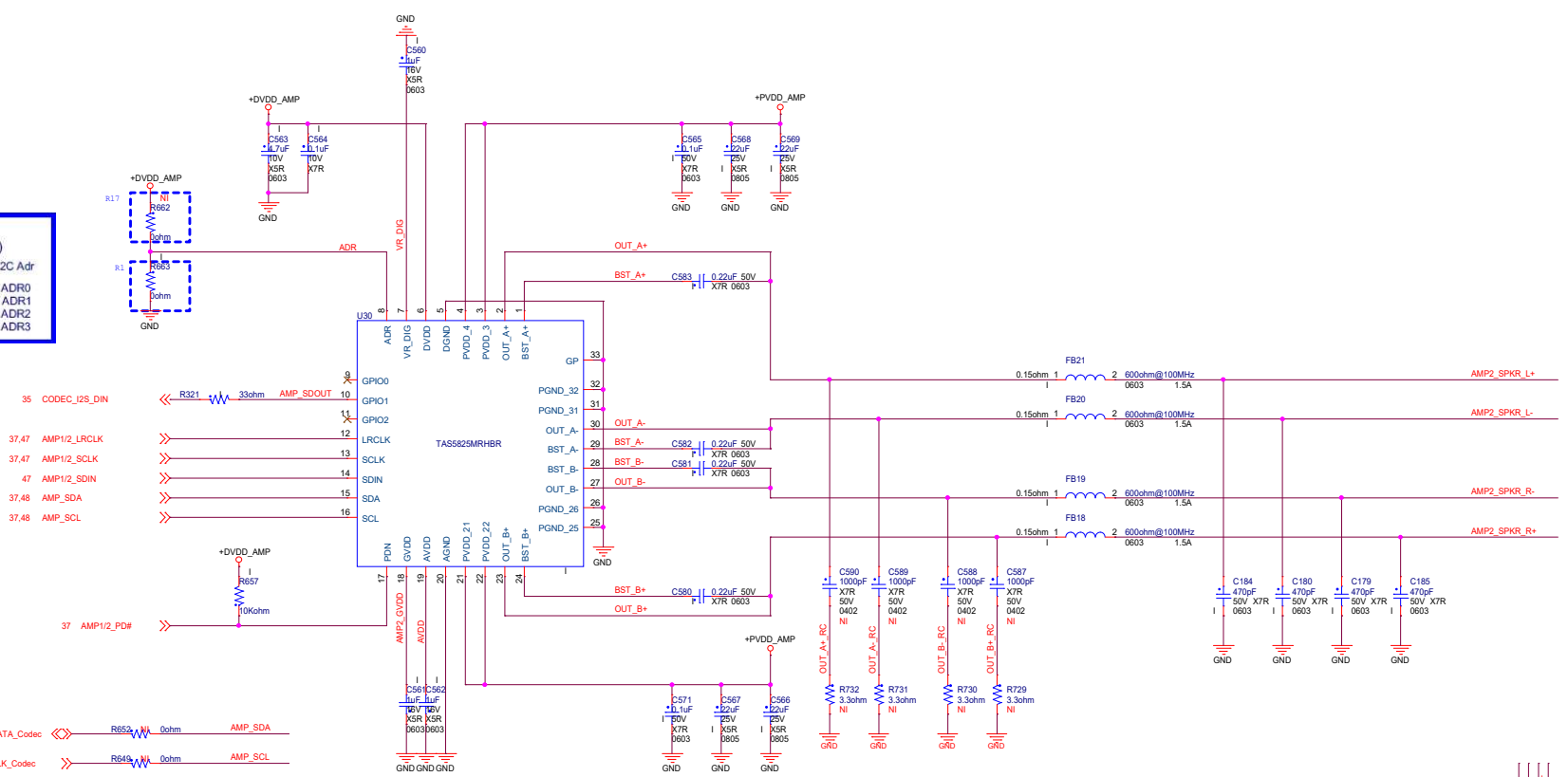


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Amp for 2nd set SPKER

ADR PIN Config (I2C Slave Address 0)			
R1	R17	I2C Adr	
(DEFAULT)	0 ohm	DNP	ADR0
	1k	DNP	ADR1
	4.7k	DNP	ADR2
	15k	DNP	ADR3



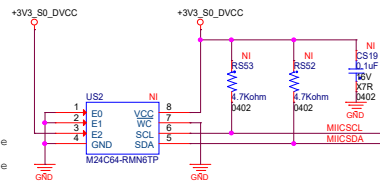
SPEAKER	
pin#	pin define
1	SPKR L+
2	SPKR L-
3	SPKR R-
4	SPKR R+

RESERVED

eDP TO LVDS - RTD2136

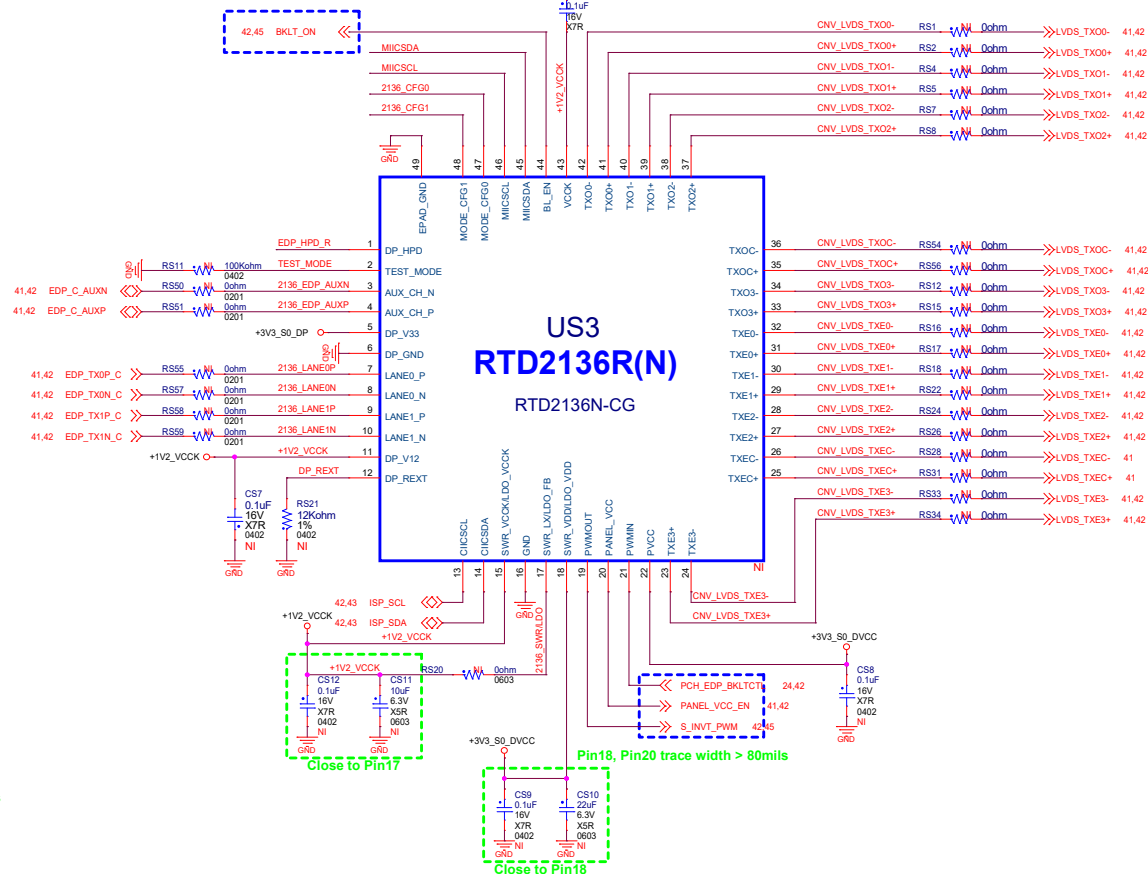
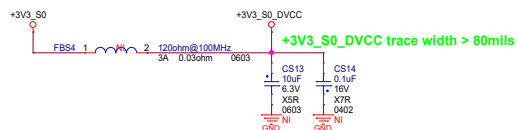
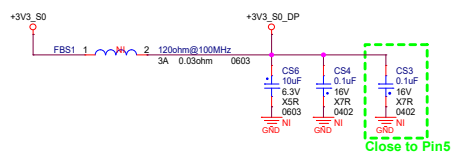
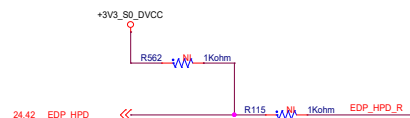
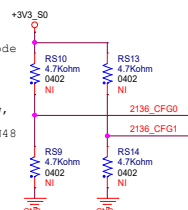
EEPROM Mode
In EEPROM mode, an additional
EEPROM is needed.
EEPROM should configure with
following condition.

- 1- EEPROM with a size 8K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8



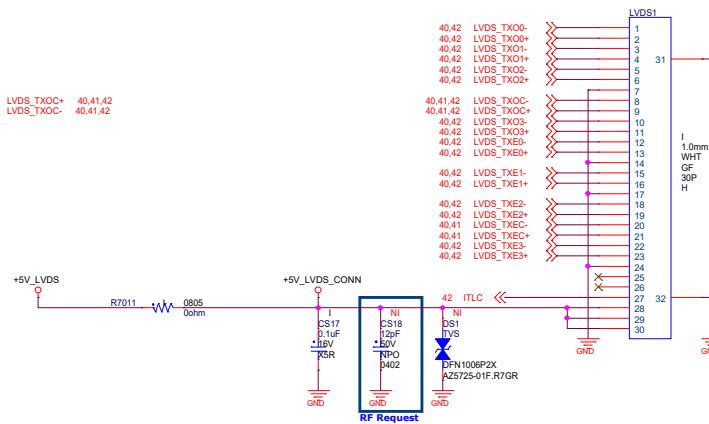
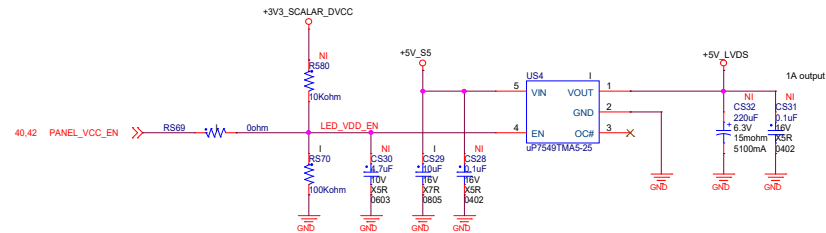
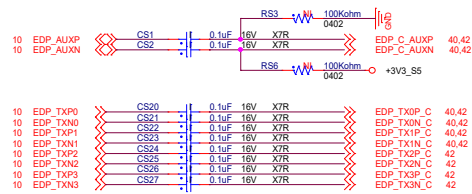
RTD2136 Supports three operation mode
for system design.
Reserved 4.7K resistor pull up/low
for mode selection

ROM ONLY Mode : PIN47 4.7K pull low,
PIN48 4.7K pull high
EP Mode : PIN47 4.7K pull high, PIN48
4.7K pull low
EEPROM Mode : PIN47 4.7K pull high,
PIN48 4.7K pull high

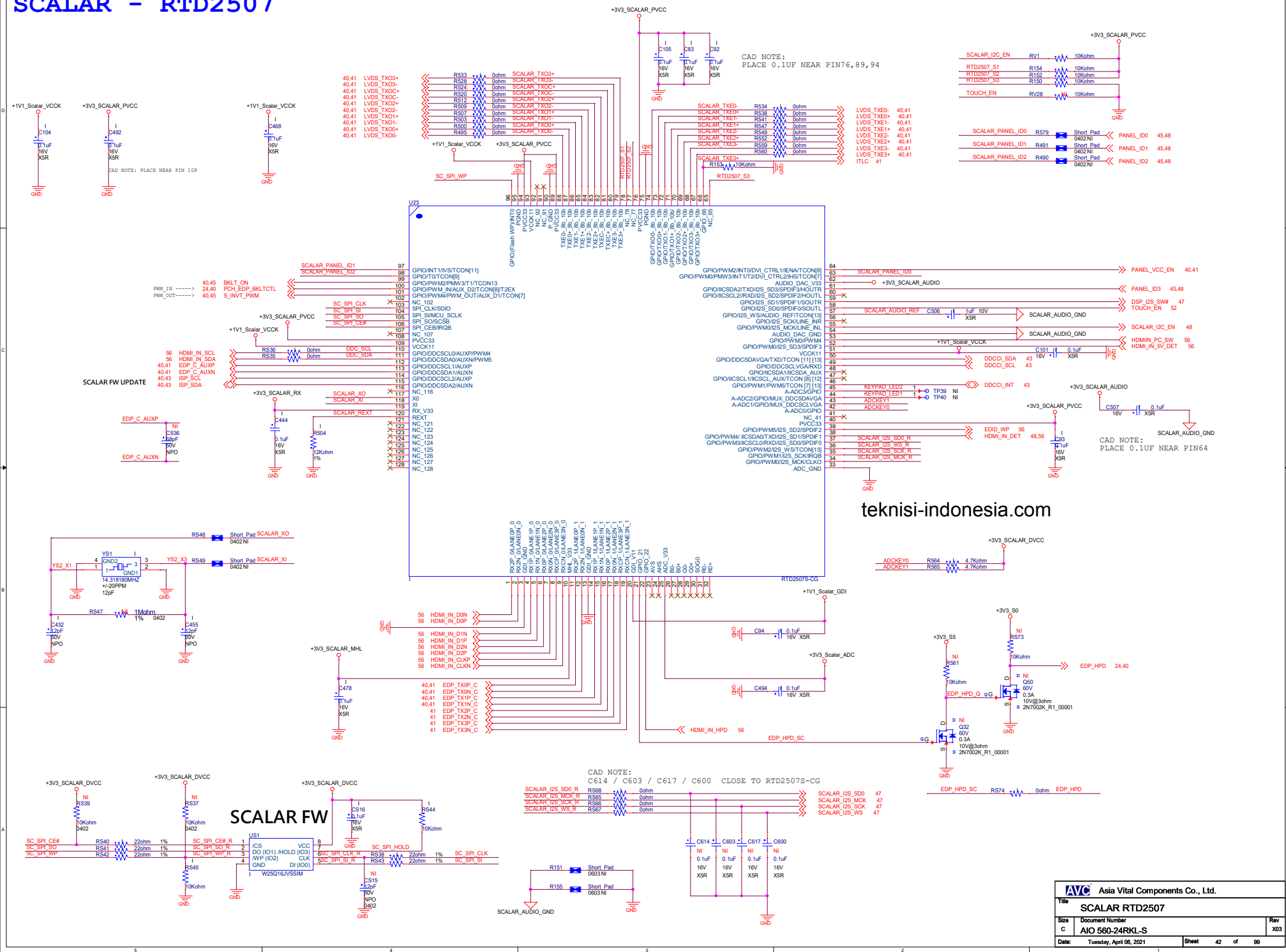


LVDS CONNECTOR

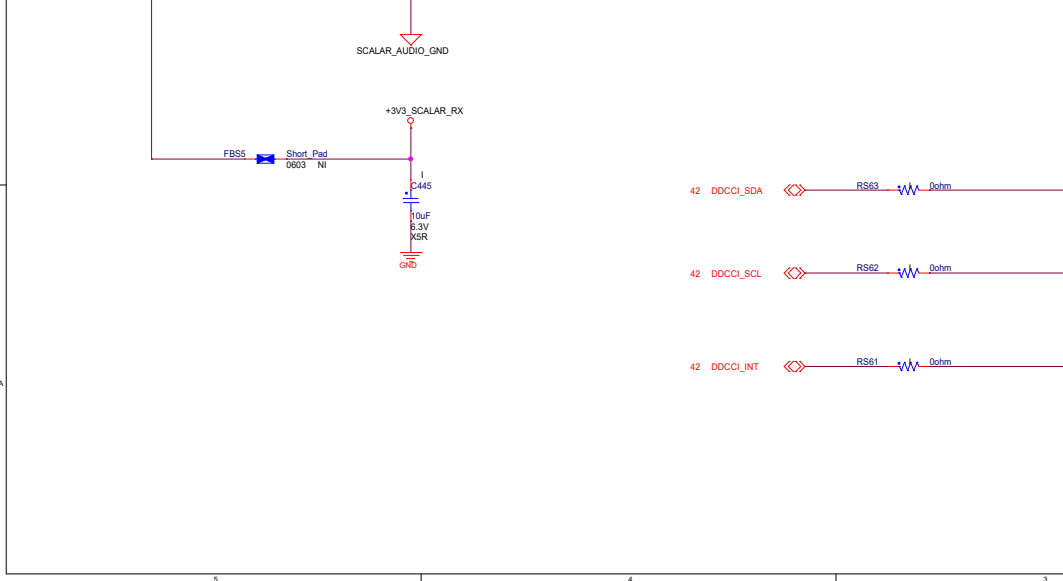
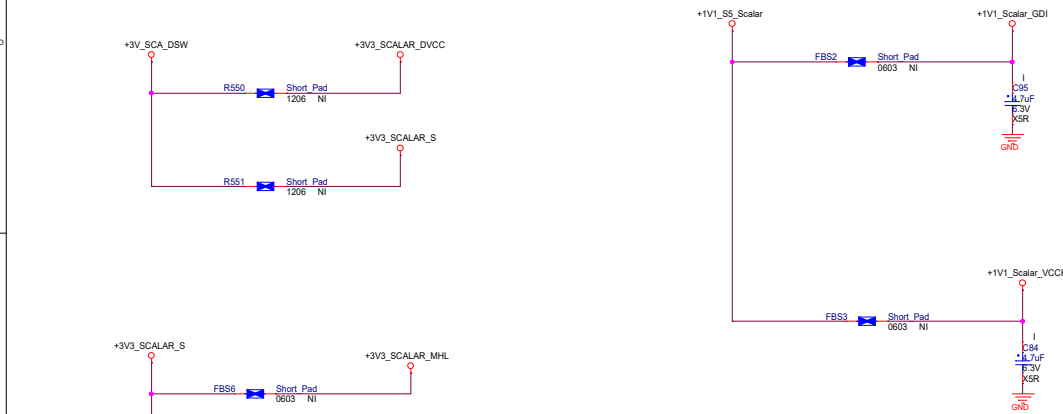
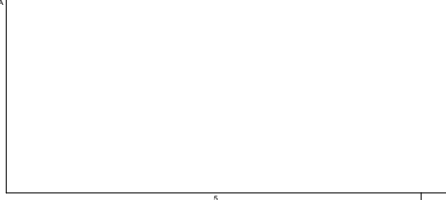
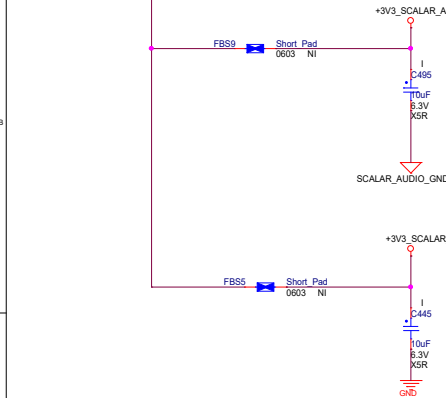
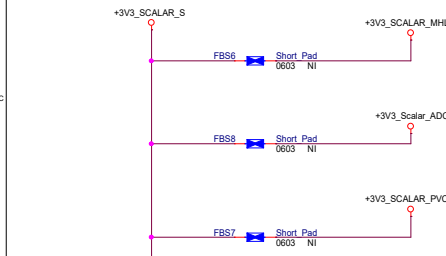
SCALAR AND CONVERT SHARE



SCALAR - RTD2507



The diagram shows the routing of the +3V3_SCALAR_DSW signal. It starts at a +3V3_SCALAR_DVCC supply, goes through a 555 ohm resistor (R550) and a short pad, then splits to a +3V3_SCALAR_S supply through a 551 ohm resistor (R551) and another short pad. A ground connection is also shown at the input node.



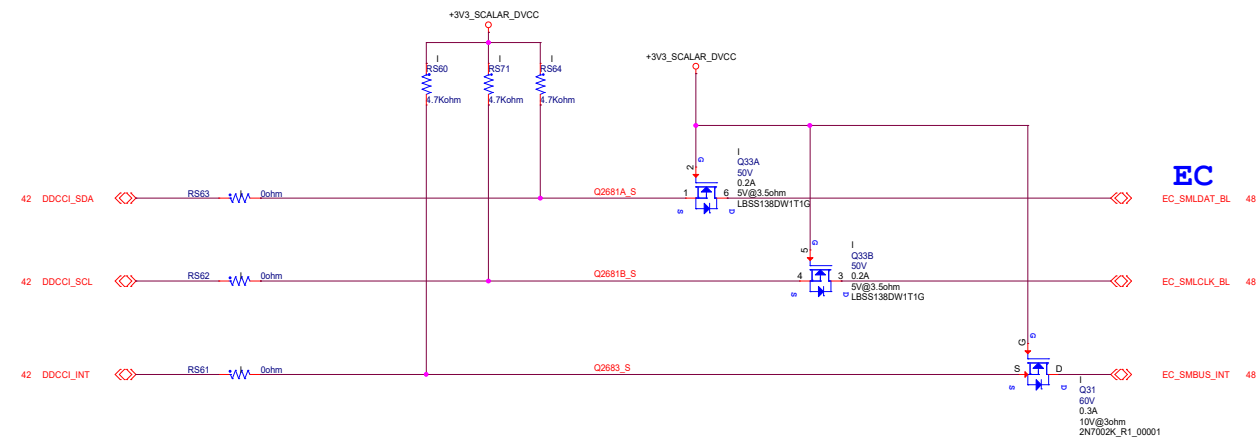
ISP_CNTL pin must keep low level anytime except ISP mode

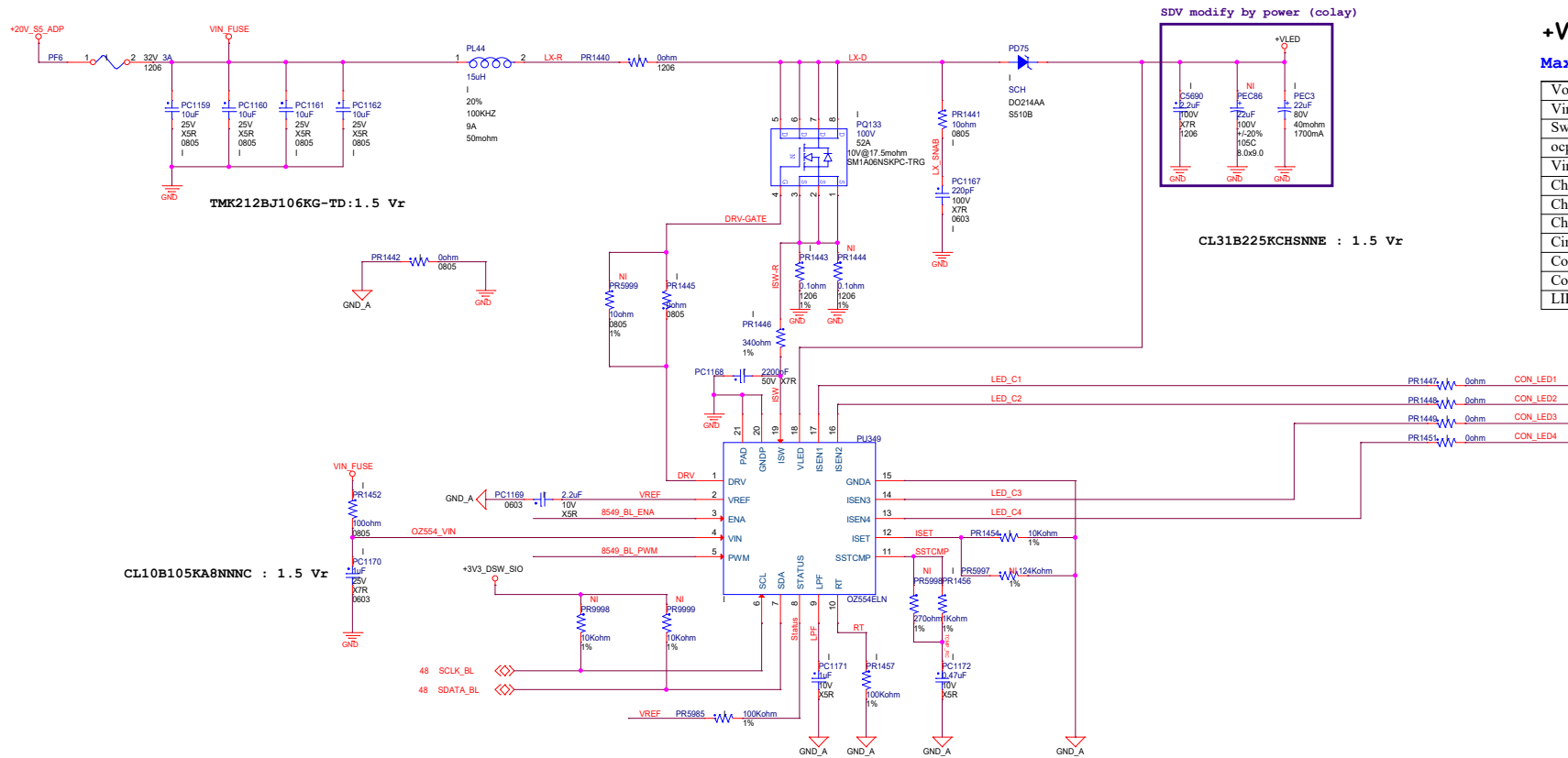
SCALAR ISP_CNTL	Mode
H	Simultaneous
L	Isolate

ISP_CNTL pin must keep low level
anytime except ISP mode

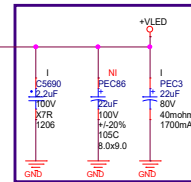
SCALAR ISP_CNTL	Mode
H	Simultaneous
L	Isolate

SCALAR DATA SYNC





SDV modify by power (colay)

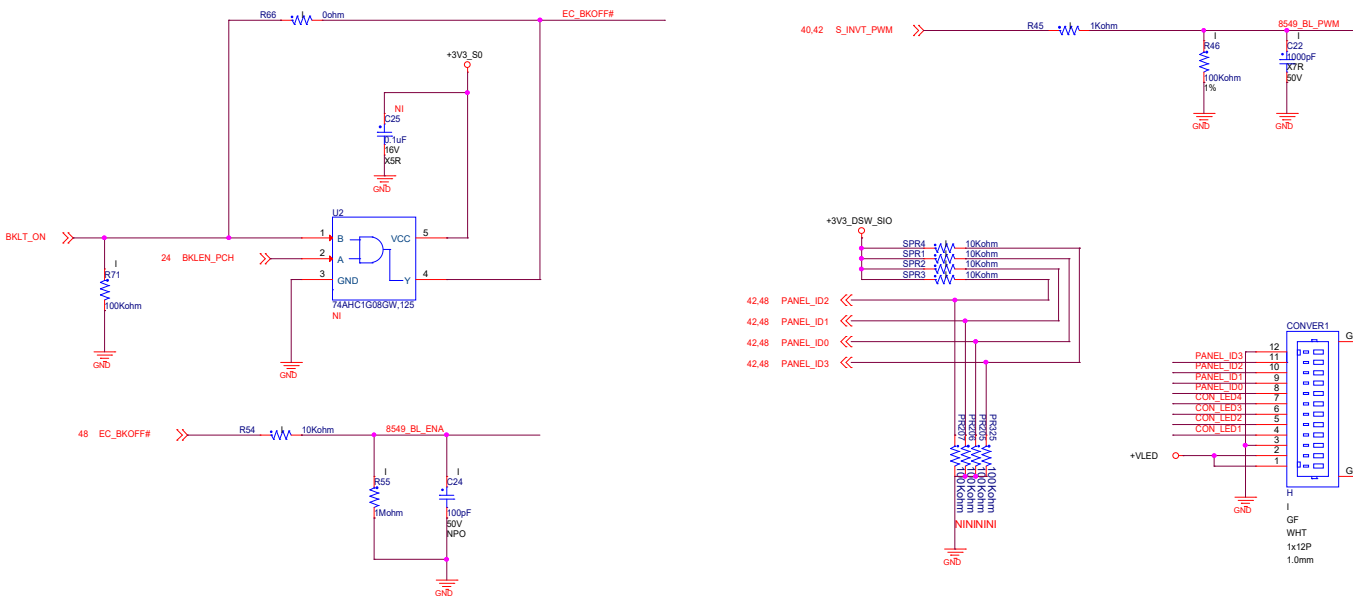


CL31B225KCHSNNE : 1.5 Vr

+VLED

Max Load:0.26A

Vout	Depend on panel
Vin	20V
Switch Freq	400KHz
ocp	3.3A
Vin_Iripple	10uFx4/1A
Choke size	22uH/7.6X7.1mm
Choke Ide/Isat	2.5A/3.8A
Choke DCR	125mohm
Cin CAP	10uFx4
Cout CAP	2.2uFx4
Cout CAP ESR	
LIR	



Converter

pin#	pin define
1	VLED
2	VLED
3	GND
4	ISEN1
5	ISEN2
6	ISEN3
7	ISEN4
8	Panel_ID0
9	Panel_ID1
10	Panel_ID2

Panel Converter ID MAP

Vendor	Panel MPN	Panel ID

AVC Asia Vital Components Co., Ltd.

Backlight OZ554ELN


Document Number: AIO 560-24RKL-S

Date: Tuesday, April 06, 2021

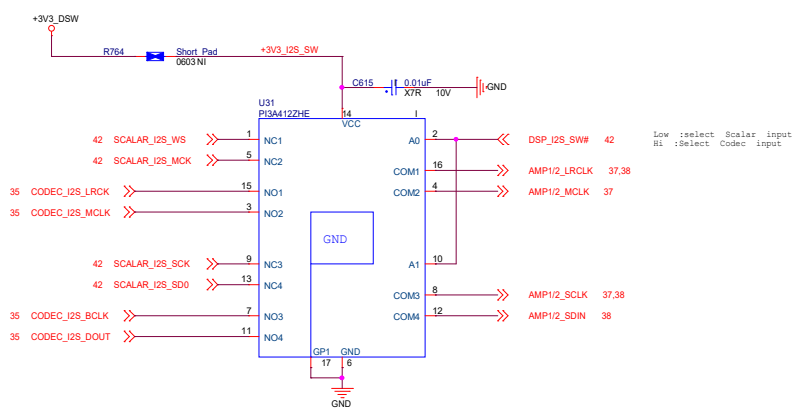
Rev: X03

Sheet: 45 of 99

RESERVED

 Asia Vital Components Co., Ltd.		
Title RESERVED		
Size C	Document Number AIO 560-24RKL-S	Rev X03
Date: Tuesday, April 06, 2021	Sheet 46	of 99

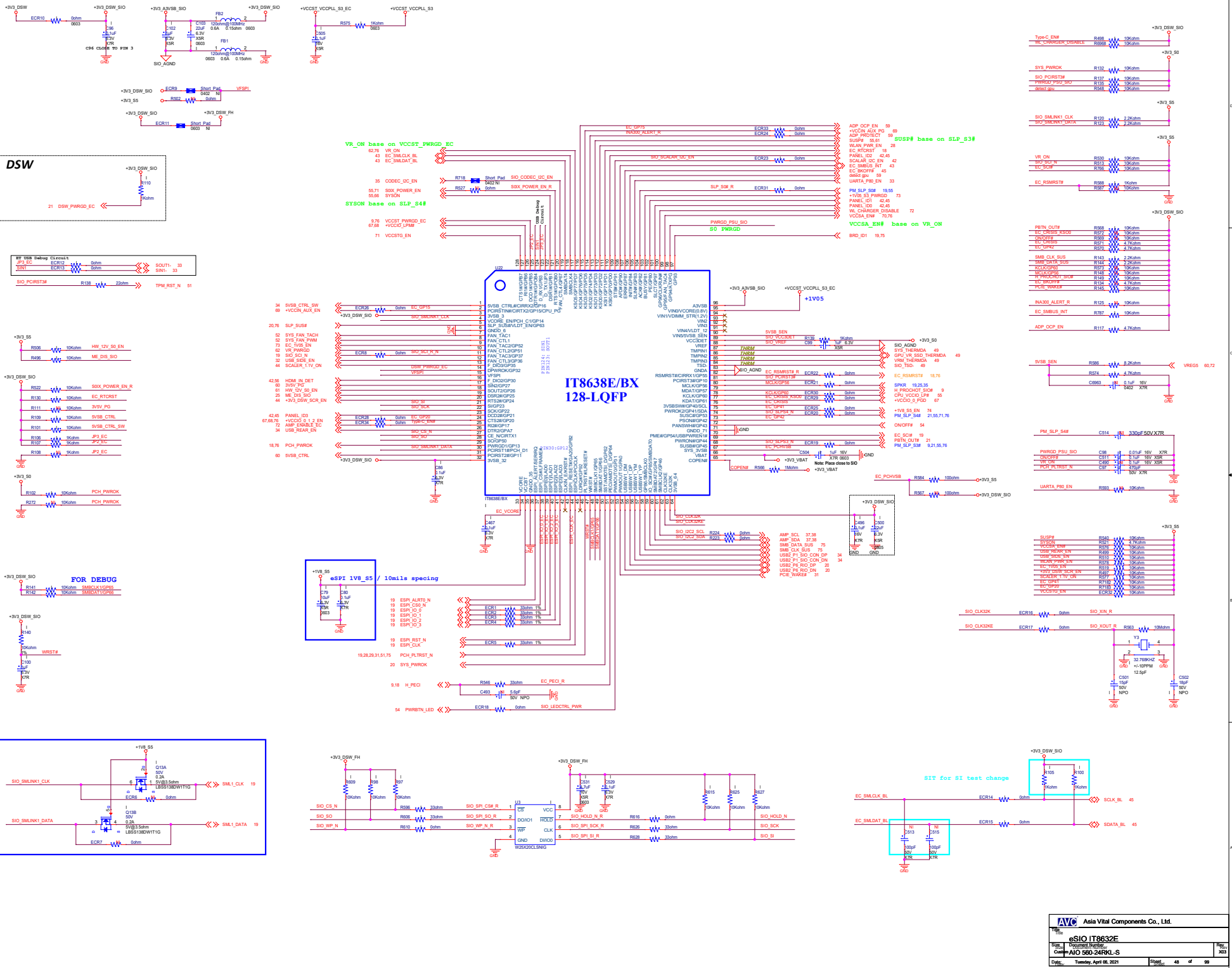
CODEC & SCALAR I2S MUX



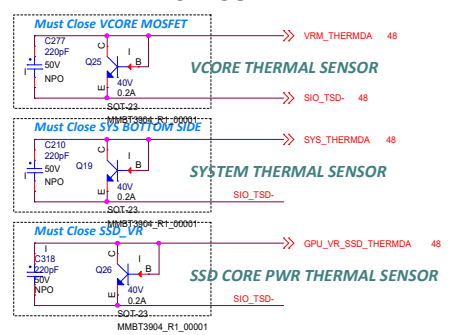
A0	Function	A1	Function
0	NC _X Connected to COM _X	0	NC _Y Connected to COM _Y
1	NO _X Connected to COM _X	1	NO _Y Connected to COM _Y

Notes:

- 1. X = 1 or 2
- 2. Y = 3 or 4

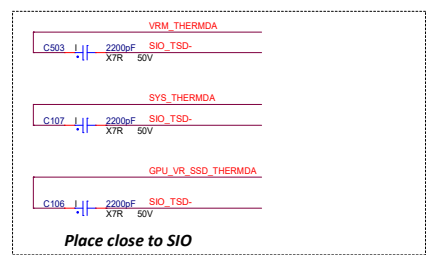


THERMAL SENSOR



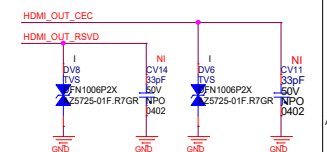
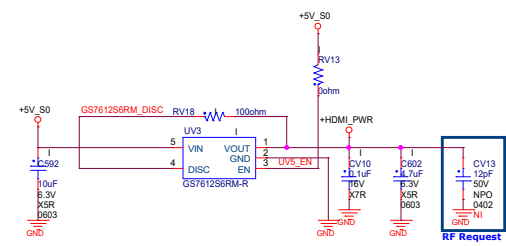
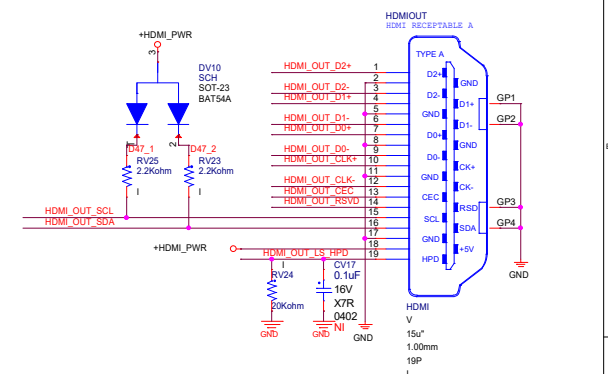
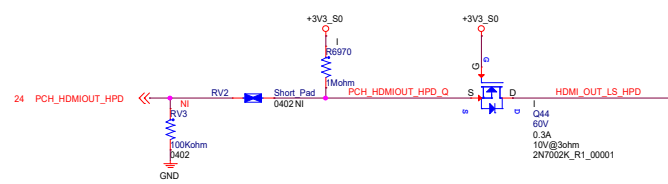
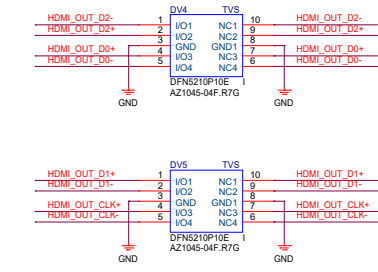
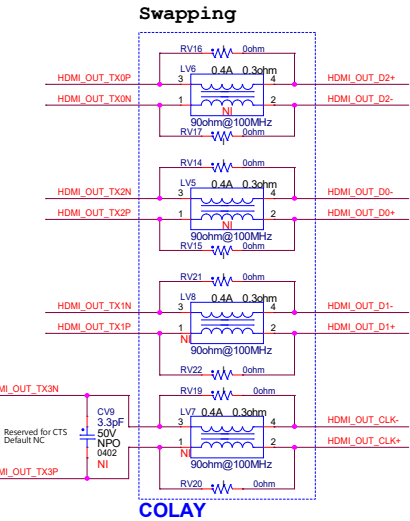
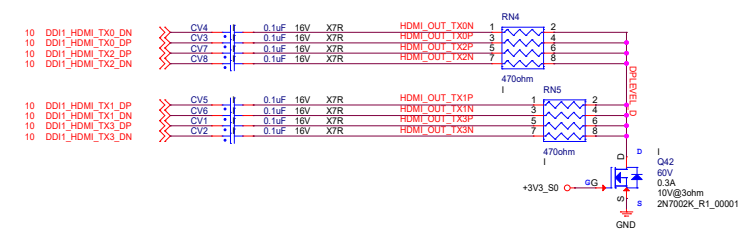
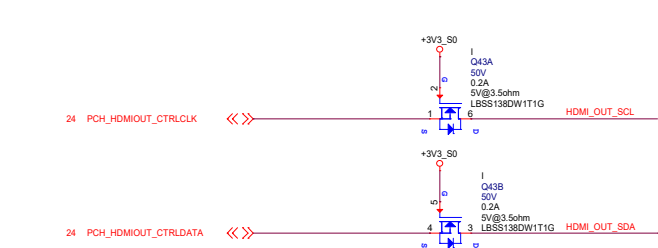
Acceptable Transistor Component
ST Micro: MMBT3904
ON Semiconductor: MMBT3904LT1
Fairchild Semiconductor: MMBT3904FSCT

CAD NOTE : Place MLCC Close to Thermal Diode

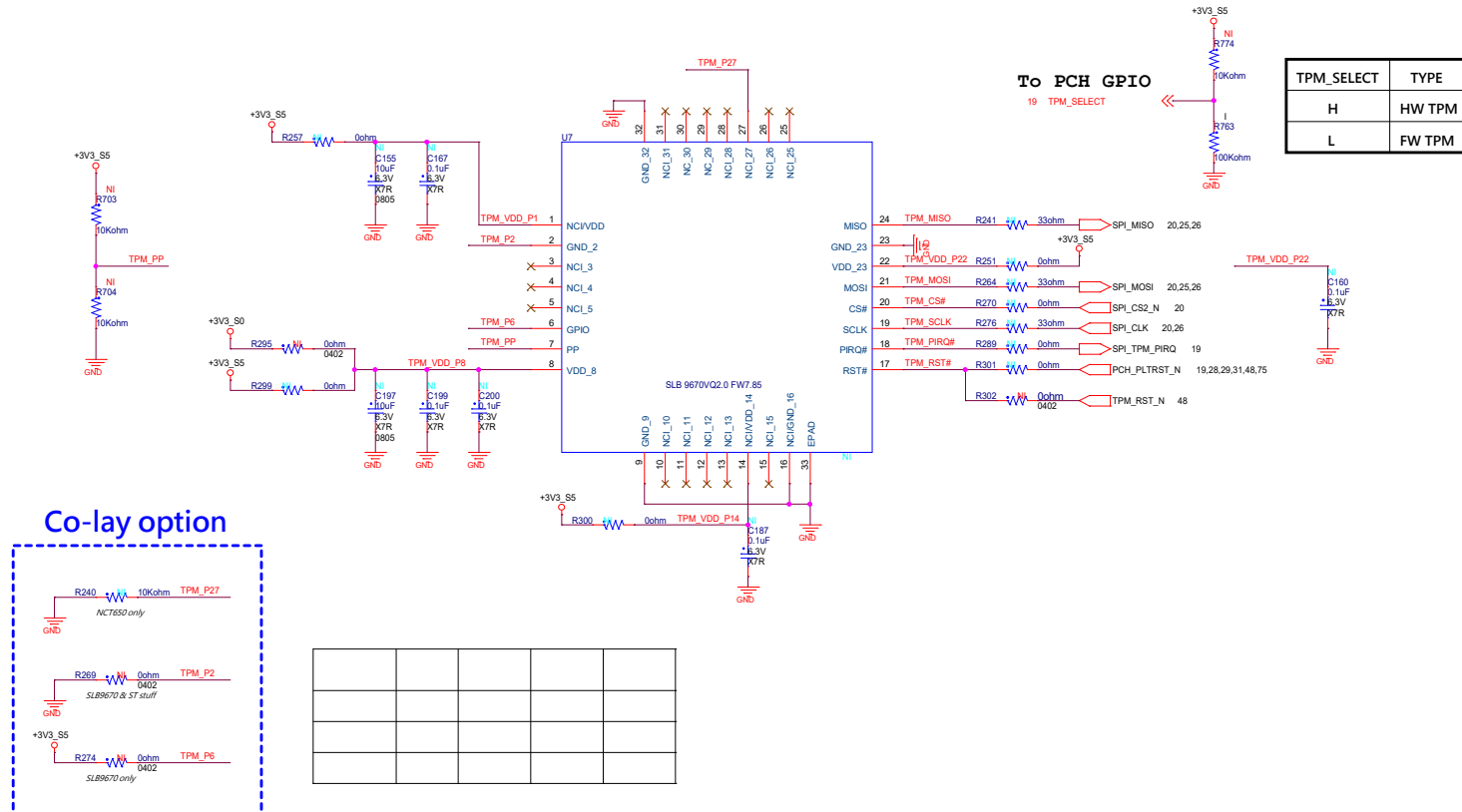


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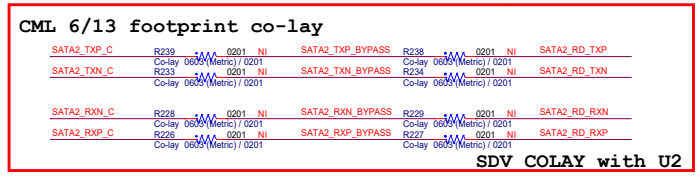
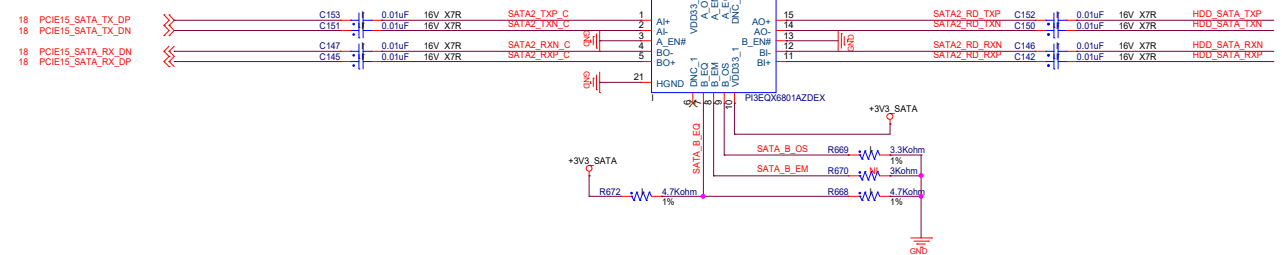
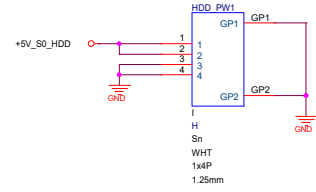
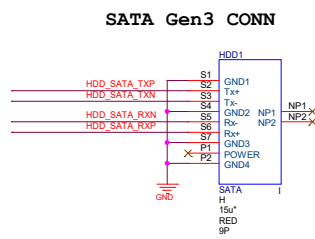
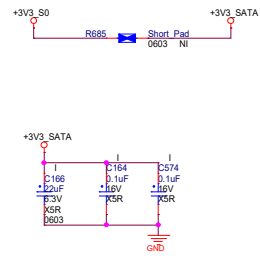
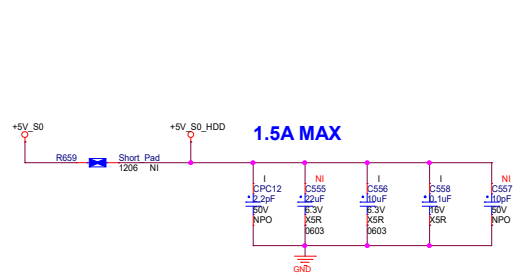
HDMI OUT



TPM 2.0



2.5" HDD



PIN CONFIGURATION for CONTROL

PIN NAME	PIN FUNCTION DESCRIPTION	Control Configuration										
A_EN# B_EN#	With Internal 200k-ohm pull-down resistor Low: Normal Operation High: Power Down Mode	For real application, they could be OPEN.										
A_EQ B_EQ	Input Equalization Tri-level Input	Equalization is controlled by PIN7&PIN17 <table><tr><th colspan="2">Input Equalization for Channel A&B</th></tr><tr><th colspan="2">Input Equalization3.0Gb/s</th></tr><tr><td>0</td><td>8dB (A&B-CH)</td></tr><tr><td>1</td><td>16dB (A&B-CH)</td></tr><tr><td>Vdd/2</td><td>4dB (A&B-CH)</td></tr></table>	Input Equalization for Channel A&B		Input Equalization3.0Gb/s		0	8dB (A&B-CH)	1	16dB (A&B-CH)	Vdd/2	4dB (A&B-CH)
Input Equalization for Channel A&B												
Input Equalization3.0Gb/s												
0	8dB (A&B-CH)											
1	16dB (A&B-CH)											
Vdd/2	4dB (A&B-CH)											
A_EM B_EM	Output Emphasis Adjustment it is analog resistive adjustment. please refer to the next row table	Emphasis is controlled by PIN4&13, PIN5&12 and PIN6&11 of SW1 for Channel A, PIN4&13, PIN5&12 and PIN6&11 of SW2 for Channel B, <table><tr><th colspan="2">Pre-emphasis for Channel A&B</th></tr><tr><td>PIN4&13 is open</td><td>0dB</td></tr><tr><td>PIN4&13 1s short(14k RES)</td><td>+2.0dB</td></tr><tr><td>PIN5&12 1s short(10k RES)</td><td>+3.0dB</td></tr><tr><td>PIN6&11 1s short(6k RES)</td><td>+4.0dB</td></tr></table>	Pre-emphasis for Channel A&B		PIN4&13 is open	0dB	PIN4&13 1s short(14k RES)	+2.0dB	PIN5&12 1s short(10k RES)	+3.0dB	PIN6&11 1s short(6k RES)	+4.0dB
Pre-emphasis for Channel A&B												
PIN4&13 is open	0dB											
PIN4&13 1s short(14k RES)	+2.0dB											
PIN5&12 1s short(10k RES)	+3.0dB											
PIN6&11 1s short(6k RES)	+4.0dB											
A_OS B_OS	Output Swing Adjustment it is analog resistive adjustment. please refer to the next row table	Swing is controlled by PIN1&16, PIN2&15 and PIN3&14 of SW1 for Channel A, PIN1&16, PIN2&15 and PIN3&14 of SW2 for Channel B, <table><tr><th colspan="2">Swing Output for Channel A&B (mV, V_{TX-DIFF-P} at 6.0Gb/s)</th></tr><tr><td>PIN1&16 is short(5k RES)</td><td>600</td></tr><tr><td>PIN2&15 is short(4k RES)</td><td>820</td></tr><tr><td>PIN3&14 is short(2k RES)</td><td>1200</td></tr></table>	Swing Output for Channel A&B (mV, V _{TX-DIFF-P} at 6.0Gb/s)		PIN1&16 is short(5k RES)	600	PIN2&15 is short(4k RES)	820	PIN3&14 is short(2k RES)	1200		
Swing Output for Channel A&B (mV, V _{TX-DIFF-P} at 6.0Gb/s)												
PIN1&16 is short(5k RES)	600											
PIN2&15 is short(4k RES)	820											
PIN3&14 is short(2k RES)	1200											
PIN6&16 PIN10&20	Voltage PIN	PI3EQX6801A2DE (3.3V)@TQFN20: PIN10&20=VDD33 (3.3V), PIN6&16=DNC										

Receive Equalizer Configuration Table

x_EN#	x_EQ	Input Equalization @ 3.0GHz	Function
1	X	N/A	Channel x disabled, Hi-impedance terminations
0	0	8dB	Channel enabled, medium input equalization
0	1	16dB	Channel enabled, high input equalization
0	V _{DD} /2	4dB (Default)	Channel enabled, low input equalization

Output Swing Adjustment (1)

R[A:B]_OS (Ω)	Output Swing, mV (V _{TX-DIFF-P}) ⁽²⁾	
	3Gbps	6Gbps
5.5K	450	600
5K	490	660
4.5K	540	730
4K	600	820
3.5K	670	910
3K	760	1,000
2.5K	870	1,080
2K	990	1,200

Output Emphasis Adjustment (1, 2)

R[A:B]_EM (Ω)	Pre-emphasis
Do Not Connect	0dB
14K	+2.0dB
10K	+3.0dB
6K	+4.0dB
2K	+6.0dB

Note:
1. Suggested initial test values. Exact resistor values will vary depending on PCB design.
2. Referenced to output saving of 600mV, will vary as a function of swing, increasing as swing decreases.

Note:
V_{MAX} of output can not exceed 1,200mVpp (i.e. V_{DIFF-PRE} can not exceed 1,200mV)

Note:
1. Suggested initial test values. Exact resistor values will vary depending on PCB design.
2. Auto HDD Rate Detection is ON.

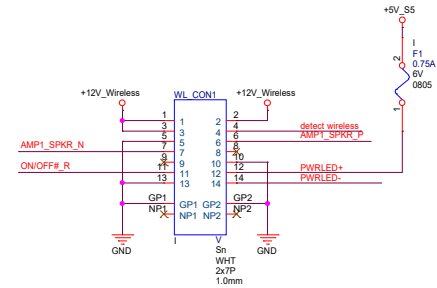
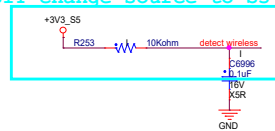
Asia Vital Components Co., Ltd.

Title: SATA 3.0	
Size: C	Document Number: AIO 560-24RKL-S
Date: Tuesday, April 06, 2021	Sheet: 53 of 99

WIRELESS CHARGER CONN



SIT change source to S5

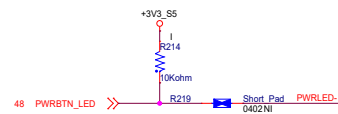


```
Id = 25mA @ 2.8V (SPEC)
Id = (5V-2.8V) / 330ohm = 5mA
5m * 3.2 V = 16 mW
LED=0.1W (For Current limit R)
```

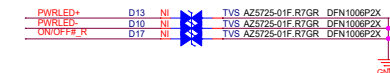
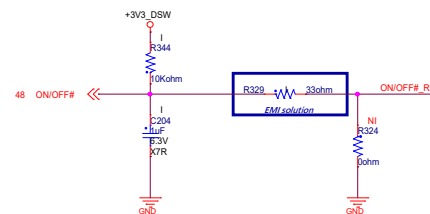
Pin #	Name	Description
1	+12V	POWER
2	+12V	POWER
3	+12V	POWER
4	GND	GND
5	GND	GND
6	AMP1_SPKR_L+	Analog output L+
7	AMP1_SPKR_L-	Analog output L-
8	AMP1_SPKR_R-	Analog output R-
9	AMP1_SPKR_R+	Analog output R+
10	GND	GND

NO.	Input Power(W)	
	no RX	RX=0A
S1	0.103	1.710
S2	0.131	1.840
Spec	<1W	<3W

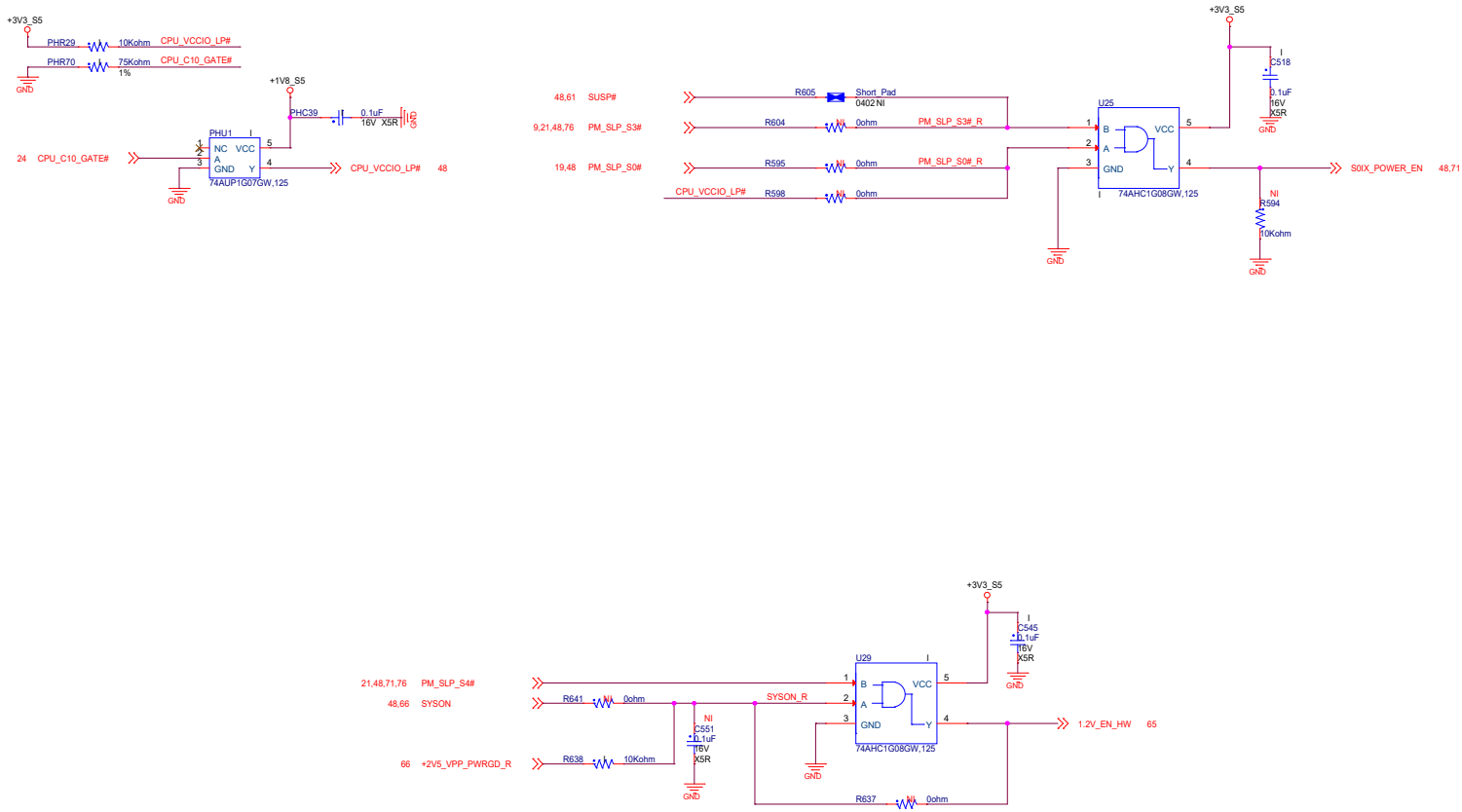
Power Button LED



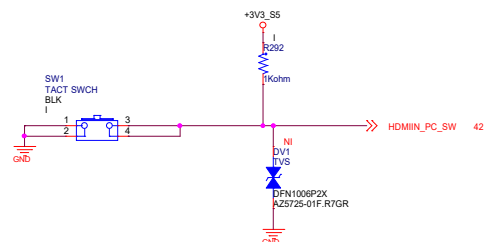
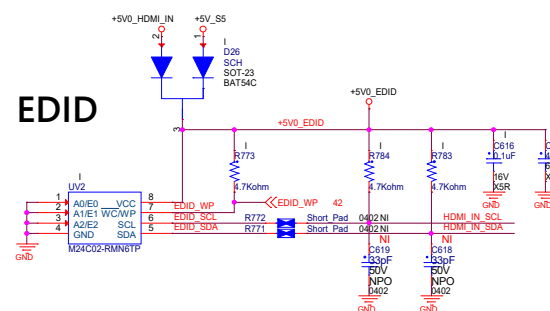
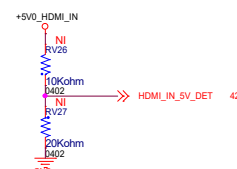
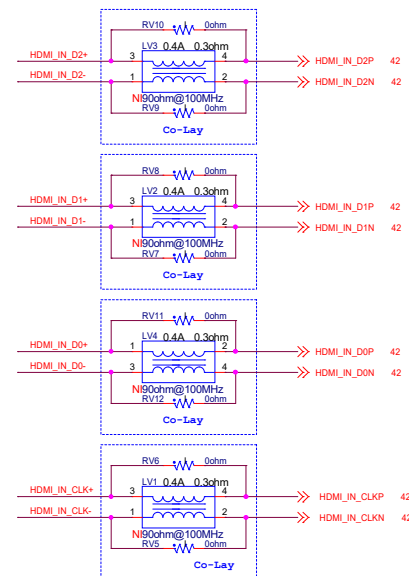
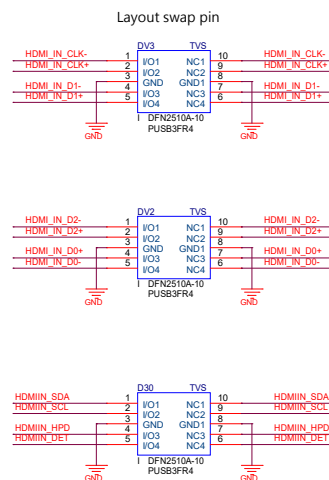
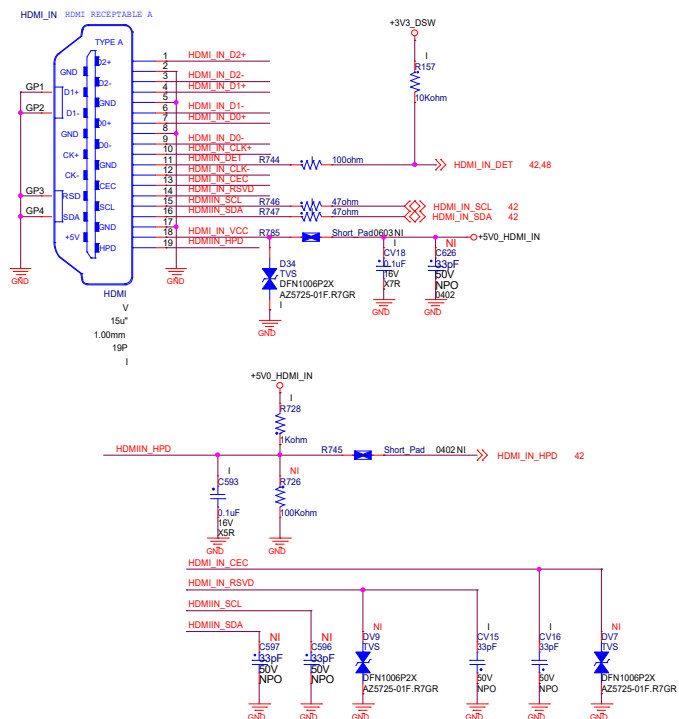
Power LED	
S0	LED is on steady WHT
S1 / S3	LED Blinks (1Hz/s)
S4 / S5	LED OFF



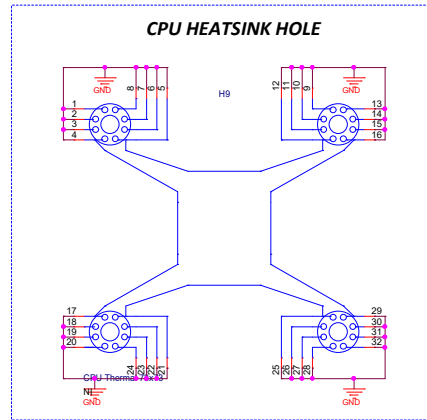
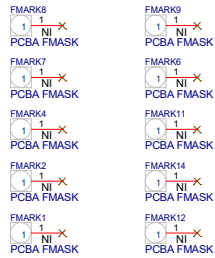
MODERN STANDBY/CEC



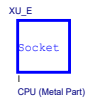
HDMI IN



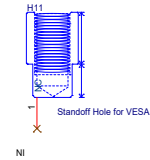
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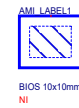
BOM-METAL



Hole for VESA



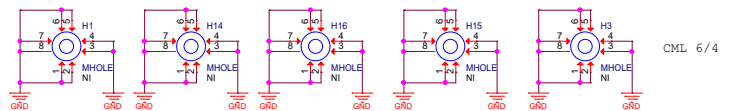
LABEL



PCB

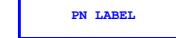


SCREW



FAN SCREW & STAND-OFF

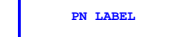
BAR CODE Label



8S Barcode 43x9mm

1

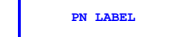
FRU Label



FRU BARCODE 42x13mm

1

LAN Label

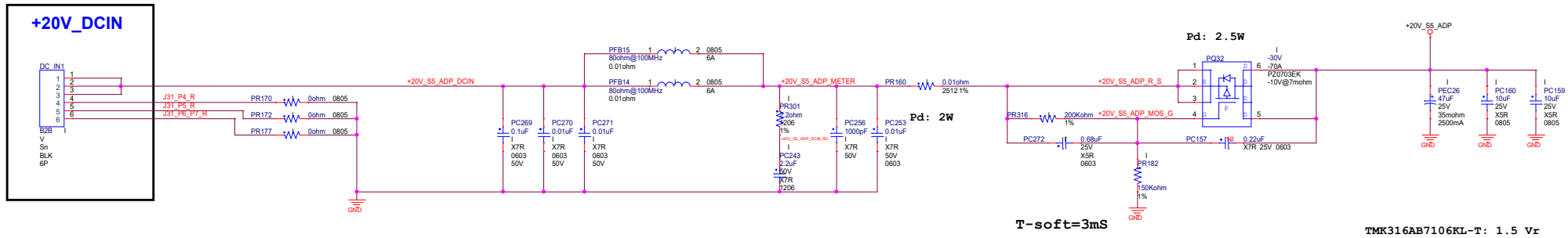


MAC Address 31x5.73mm

1

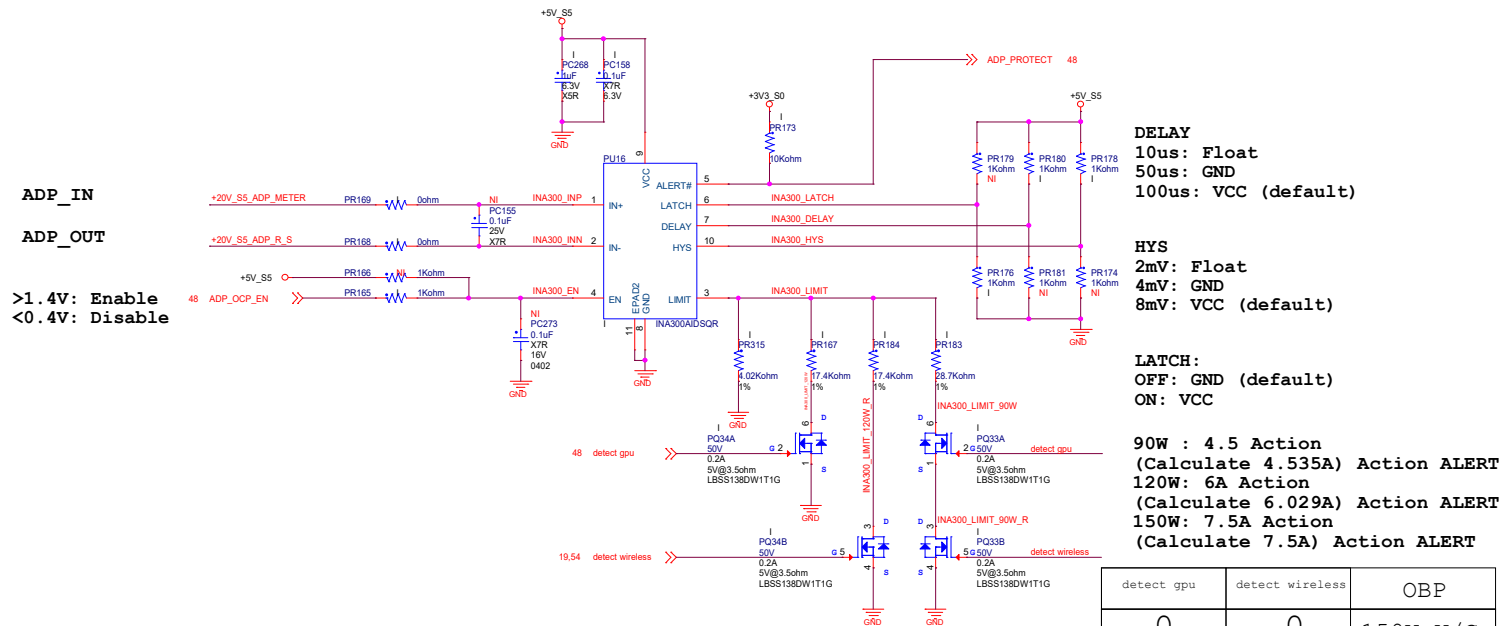
BLD Label

RESERVED



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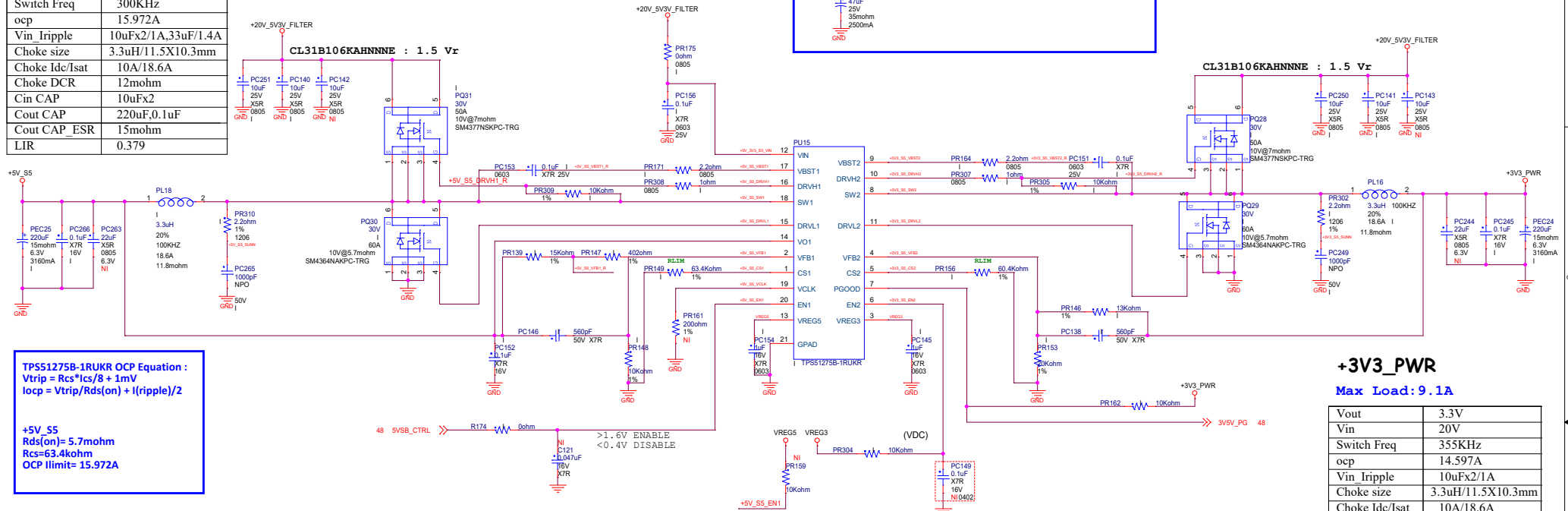
POWER METER (INA300)



+5V_S5

Max Load:10A

Vout	5V
Vin	20V
Switch Freq	300KHz
ocp	15.972A
Vin_Iripple	10uFx2/1A,33uF/1.4A
Choke size	3.3uH/11.5X10.3mm
Choke Idc/Isat	10A/18.6A
Choke DCR	12mohm
Cin CAP	10uFx2
Cout CAP	220uF,0.1uF
Cout CAP_ESR	15mohm
LIR	0.379



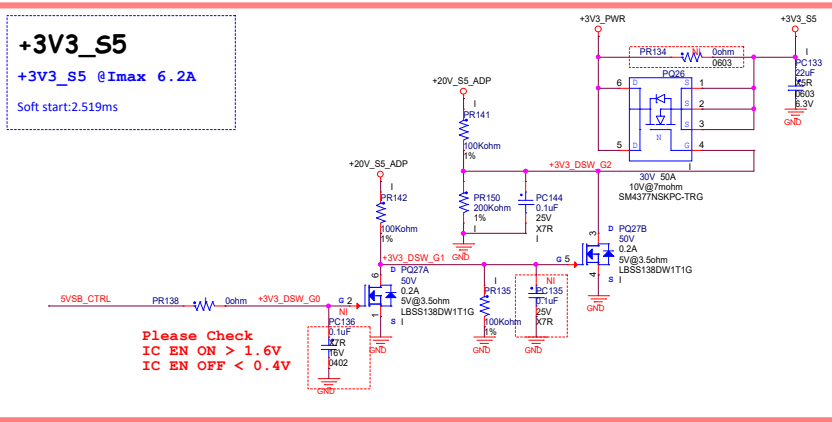
TP551275B-1RUKR OCP Equation :
 $V_{trip} = R_{cs} \cdot I_{cs} / 8 + 1mV$
 $I_{ocp} = V_{trip} / R_{ds(on)} + I_{(ripple)} / 2$

+5V_S5
 $R_{ds(on)} = 5.7mohm$
 $R_{cs} = 63.4kohm$
OCP Ilimit= 15.972A

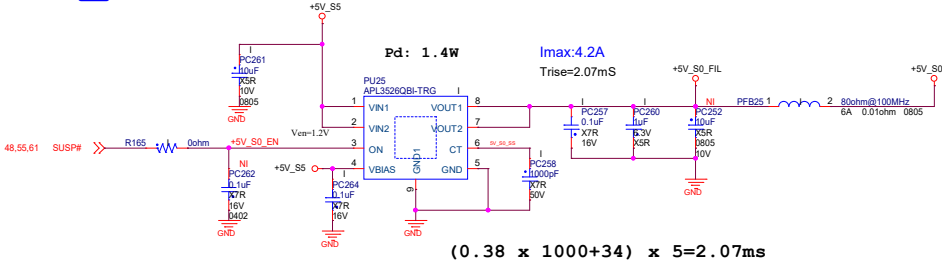
Vout	3.3V
Vin	20V
Switch Freq	355KHz
ocp	14.597A
Vin_Iripple	10uFx2/1A
Choke size	3.3uH/11.5X10.3mm
Choke Idc/Isat	10A/18.6A
Choke DCR	15mohm
Cin CAP	10uFx2
Cout CAP	220uF,0.1uF
Cout CAP_ESR	12mohm
LIR	0.258

TP551275B-1RUKR OCP Equation :
 $V_{trip} = R_{cs} \cdot I_{cs} / 8 + 1mV$
 $I_{ocp} = V_{trip} / R_{ds(on)} + I_{(ripple)} / 2$

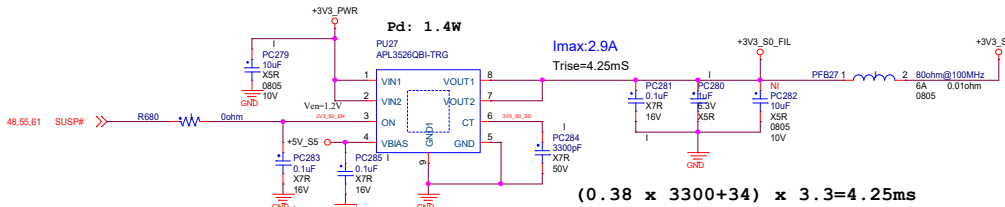
+3V3_PWR
 $R_{ds(on)} = 5.7mohm$
Rlimit=60.4k ohm
OCP Ilimit= 14.597A



+5V_S0

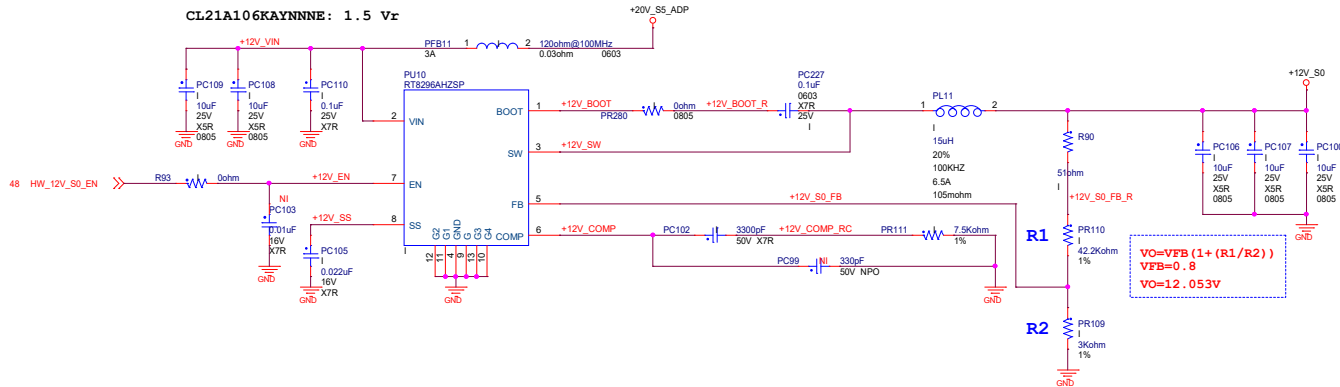


+3V3_S0

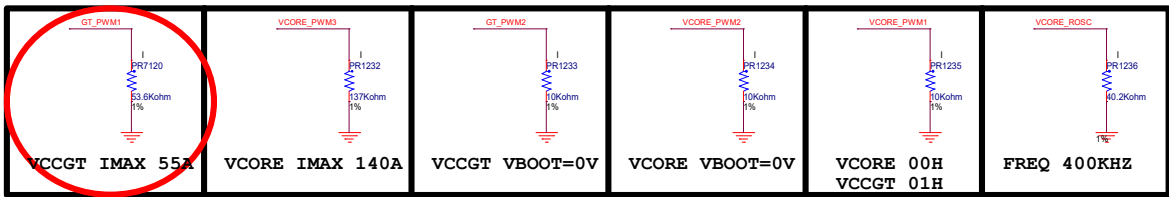
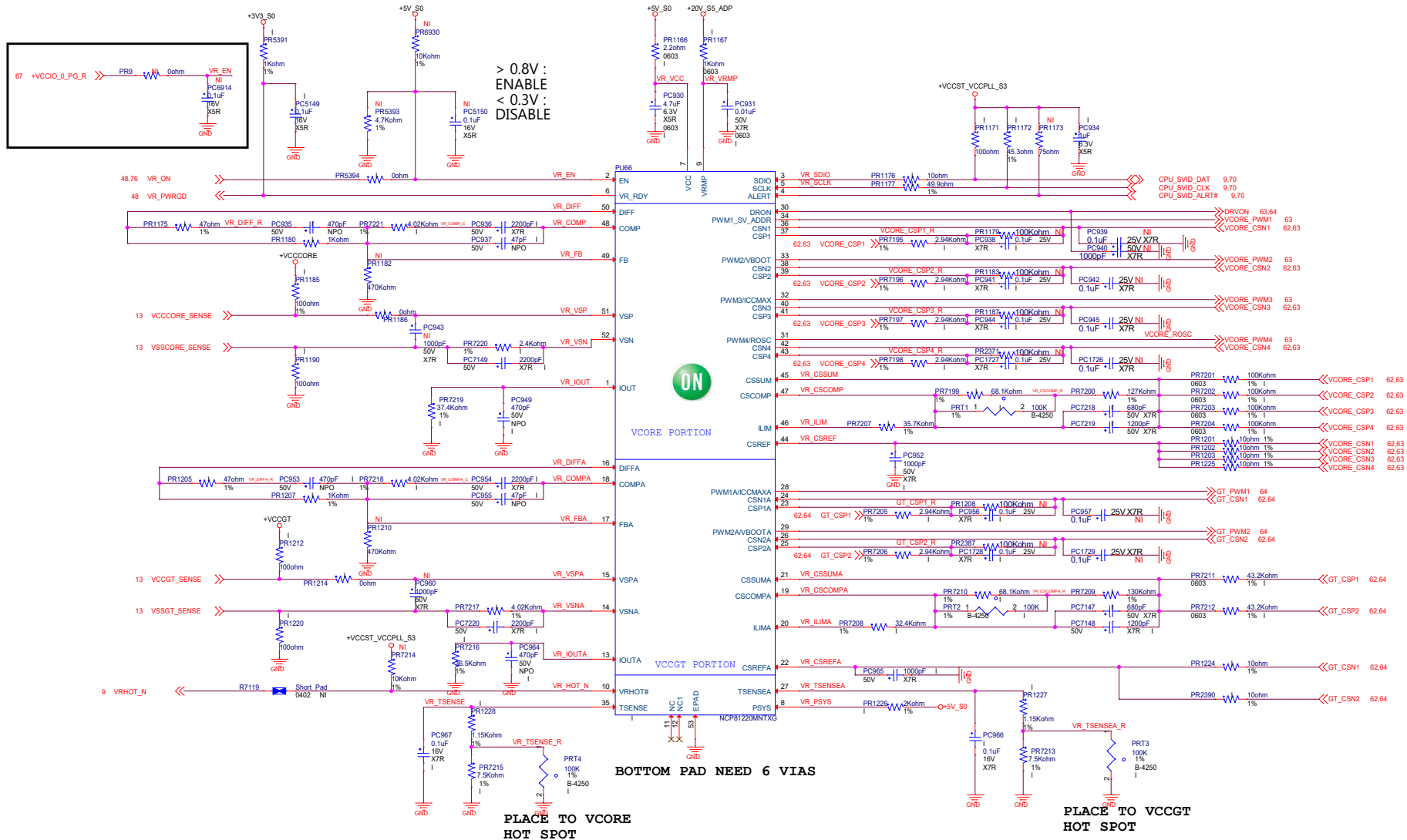


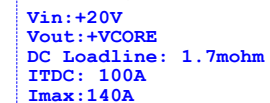
+12V_S0

Max Load:0.7A

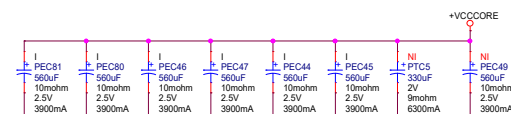
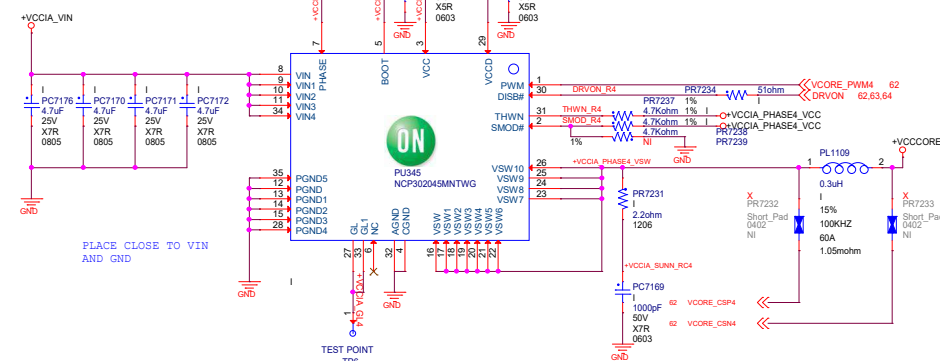


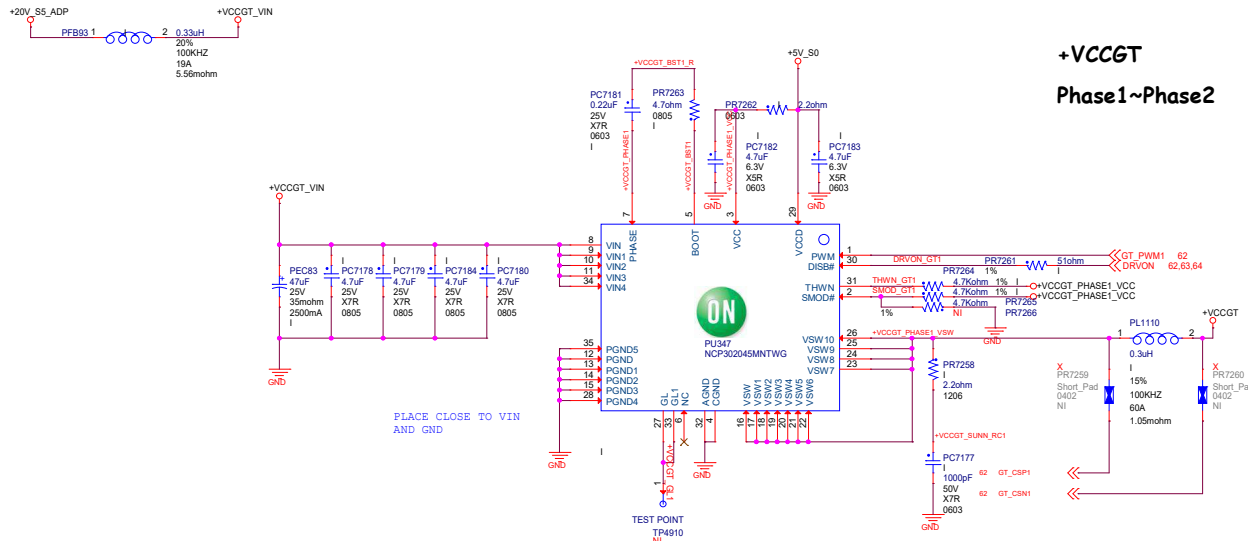
Vout	12V
Vin	20V
Switch Freq	340KHz
ocp	5.1A
Vin_ripple	10uF/1A
Choke size	15uH/7.6x6.8mm
Choke Ide/Isat	3A/6.5A
Choke DCR	105mohm
Cin CAP	10uF,0.1uF
Cout CAP	10uFx3
Cout CAP _ESR	
LIR	





Vout	Vcore
Vin	20V
Switch Freq	400KHz
minimum oep	210A
Vin Ripple	47uFx2, 2.5A, 10uF x10/1A
Choke size	0.3uH/11X7.3mm
Choke Idc/Isat	30A/60A
Choke DCR	1.05mohm
Cin CAP	47uF x2, 10uF x10
Cout CAP	560uF x6
Cout CAP ESR	10mohm x 6
LIR	

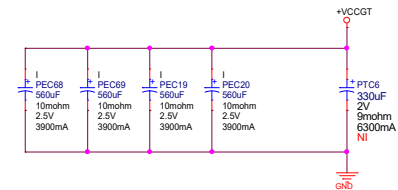
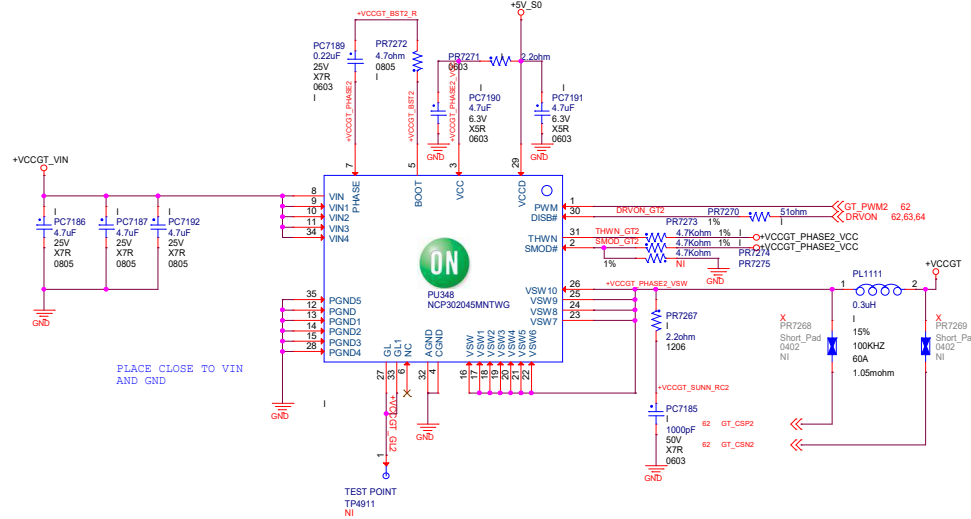




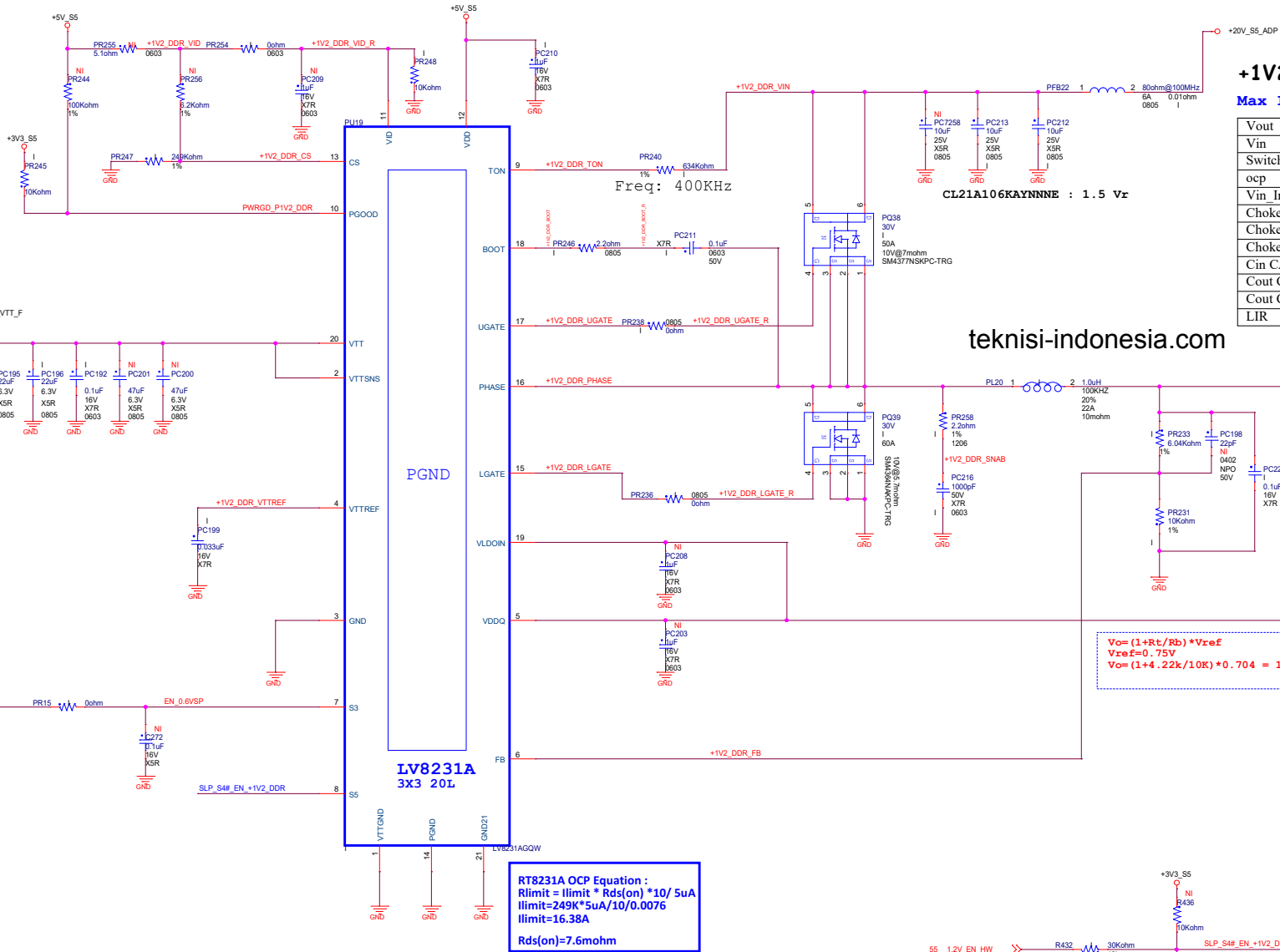
+VCCGT Phase1~Phase2

+VCCGT	
Vin: +20V	
Vout: +VCCGT	
DC Loadline: 4mohm	
ITDC: 46A	
I _{max} : 55A	

Vout	VCCGT
Vin	20V
Switch Freq	400KHz
minimum ocp	82A
Vin_ripple	10uFx4/1A + 47uFx2/2.5A
Choke size	0.3uH / 11X7.3mm
Choke Idc/Isat	30A/60A
Choke DCR	1.05mohm
Cin CAP	47uF, 10uFx1
Cout CAP	560uFx4
Cout CAP_ESR	10mohm x 4
LIR	



VID	FB
HIGH	0.675V
LOW	0.75V



+1V2_DDR4_S3

Max Load:10A

Vout	1.2V
Vin	20V
Switch Freq	400KHz
ocp	16.38A
Vin_ripple	10uFx2/1A
Choke size	1.5uH/7.3X6.8mm
Choke Idc/Isat	9A/14A
Choke DCR	15mohm
Cin CAP	10uFx2
Cout CAP	220uF,22uF
Cout CAP_ESR	17mohm
LIR	0.265

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$$V_o = (1 + R_t/R_b) * V_{ref}$$
$$V_{ref} = 0.75V$$
$$V_o = (1 + 4.22k/10K) * 0.704 = 1.203 V$$

LV8231A
3X3 20L

RT8231A OCP Equation :

$$I_{limit} = I_{limit} * R_{ds(on)} * 10 / 5uA$$

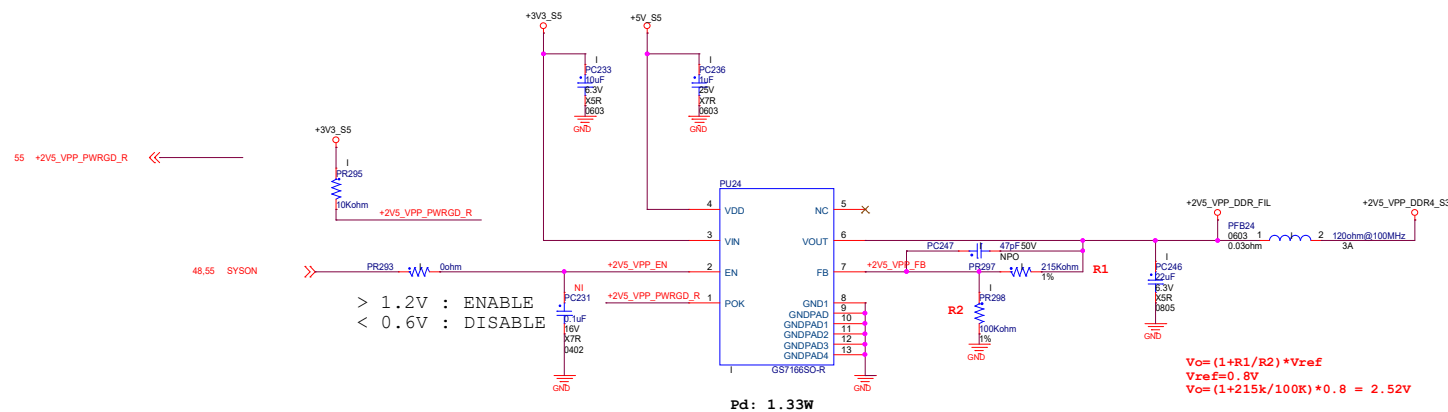
$$I_{limit} = 249K * 5uA / 10 / 0.0076$$

$$I_{limit} = 16.38A$$

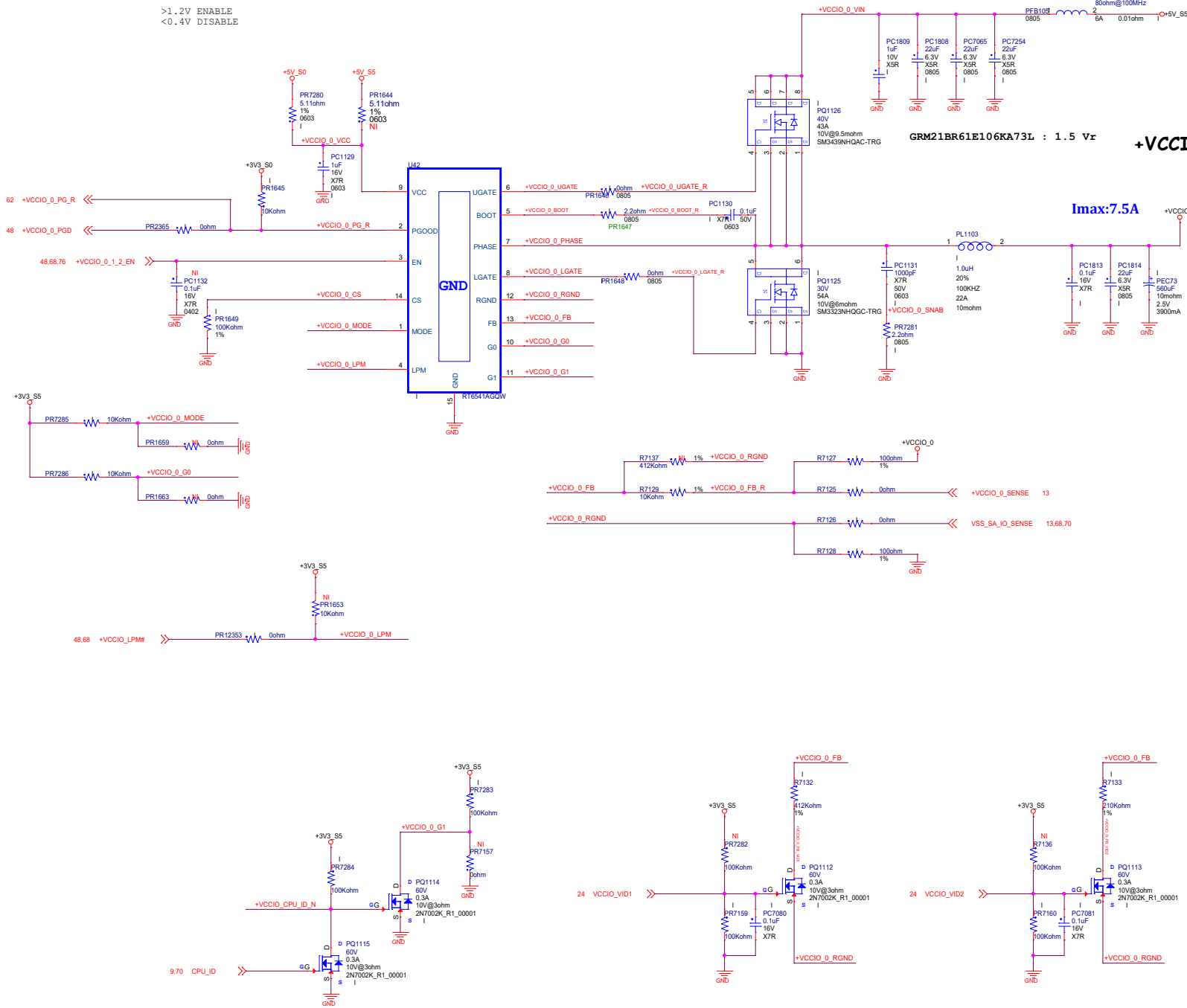
$$R_{ds(on)} = 7.6m\Omega$$

+2V5_VPP_DDR4_S3

Vin: +3V3
Vout: +2V5
Imax: 1A
OCP: 4A
Pd: 0.8W
Rja: 75
EN ON > 1.2V
EN OFF < 0.6V



>1.2V ENABLE
<0.4V DISABLE



+VCCIO_0

Vout	0.95V
Vin	5V
Switch Freq	560KHz
ocp	11.2A
Vin_ripple	10uFx2/1A
Choke size	1.0uH/7.3X6.8mm
Choke Idc/Isat	11A/22A
Choke DCR	10mohm
Cin CAP	10uFX2
Cout CAP	560uF X1
Cout CAP_ESR	10mohm
LIR	0.182

RT6541 OCP Equation :
 $V_{cs} = R_{cs} \cdot I_{cs}$
 $I_{ocp} = V_{cs} / (10 \cdot R_{ds(on)}) + \Delta I_L / 2$
 $R_{ds(on)} = 9.5 \text{ m}\Omega$
 $I_{cs} = 10 \text{ uA}$
 $\Delta I_L / 2 = 1.77 / 2 = 0.687 \text{ A}$
If Set Rlimit = 100Kohm
OCP Ilimit = 11.2A

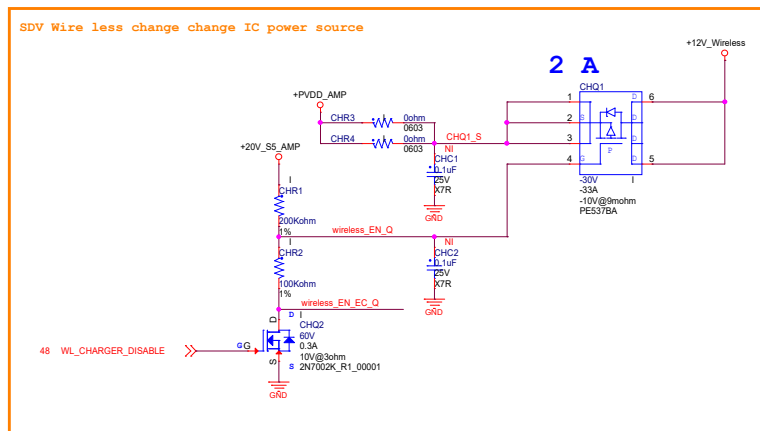
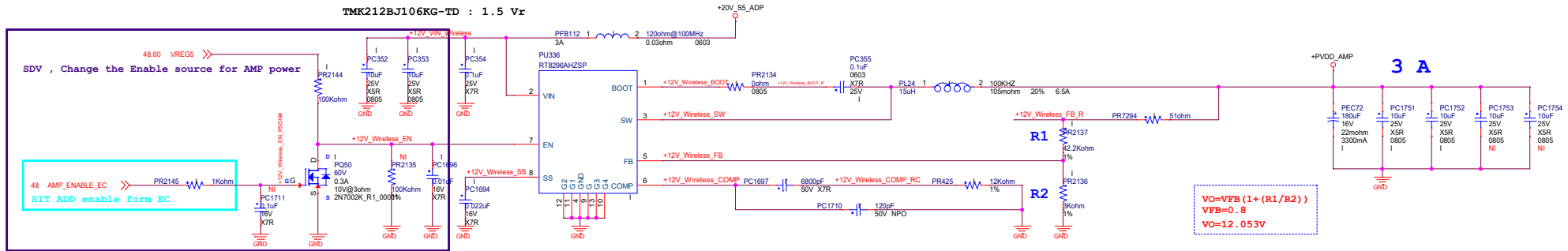
Mode logic	LPM	VID Setting		Vout (V)
		G1 logic	G0 logic	
1	0	x	x	0(LPM)
	1	0	0	0.8
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05

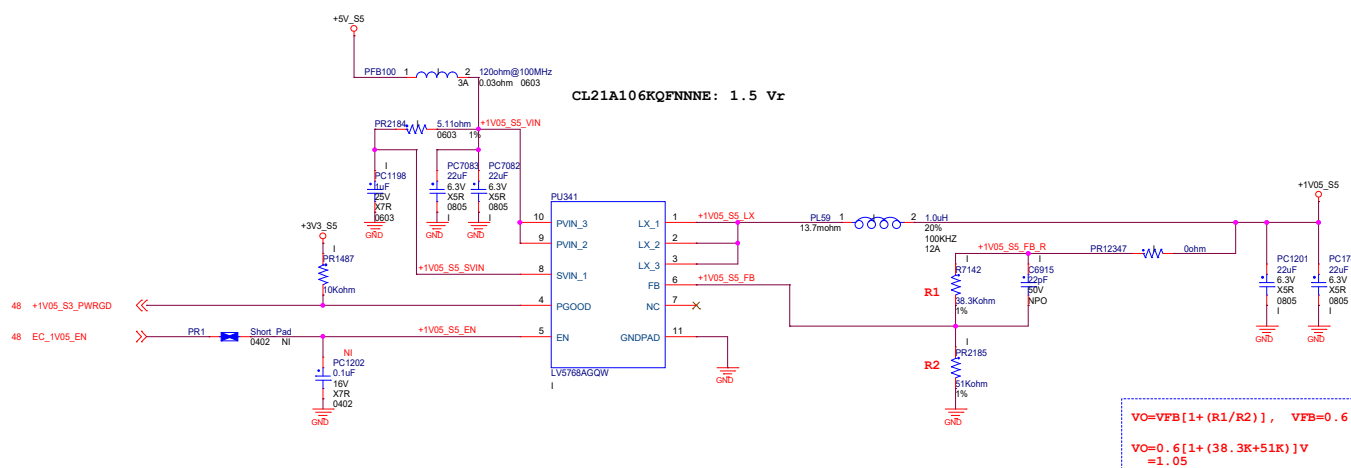
VCCIO_0_G1	VCCIO_0_VID1	VCCIO_0_VID2	Vout
Low	Low	Low	0.950V
High	Low	Low	1.050V
High	High	Low	1.075V
High	Low	High	1.100V
High	High	High	1.125V

+12V_Wireless

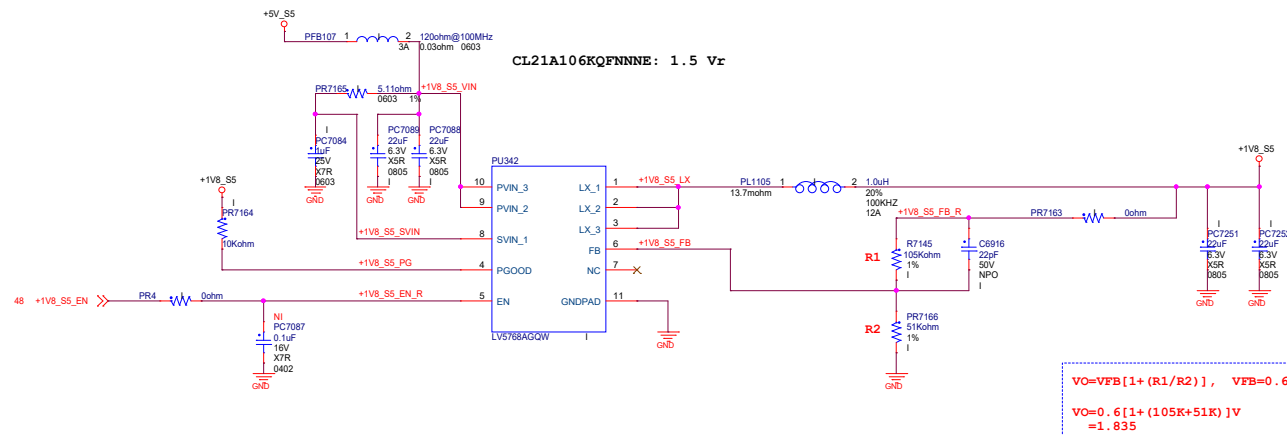
Max Load: 2A

Vout	12V
Vin	20V
Switch Freq	340KHz
ocp	5.1A
Vin_ripple	10uFx2/1A
Choke size	15uH/7.6x6.8mm
Choke Idc/Isat	3A/6.5A
Choke DCR	105mohm
Cin CAP	10uFx2,0.1uF
Cout CAP	10uFx3
Cout CAP_ESR	
LIR	





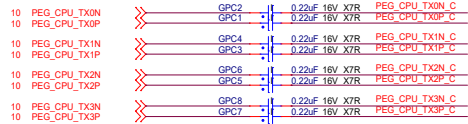
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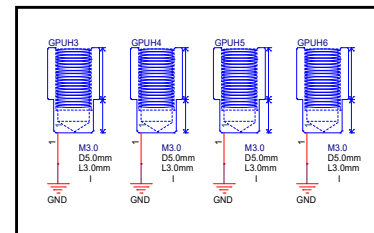
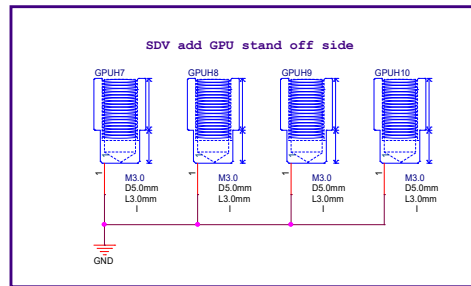
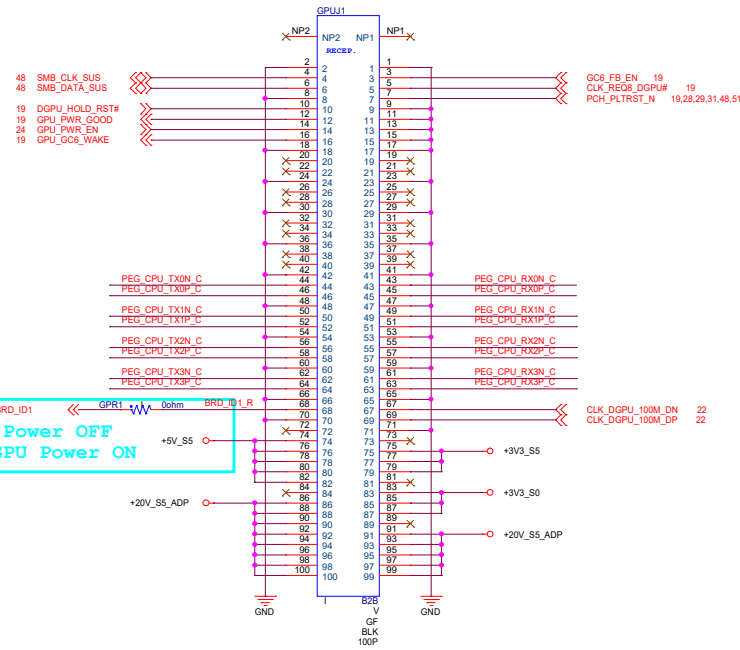
Max Load:2A CONVERTER

Vout	1.8V
Vin	5V
Switch Freq	1MHz
ocp	6A (Fixed)
Vin_Ripple	10uF/1A
Choke size	2.2uH / 5.5x5.0mm
Choke DCR	35mohm
Cin CAP	22uF
Cout CAP	10uF x2
Cout CAP_ESR	
LIR	


CPU TX




19.48 BRD_ID1 << GPR1 0ohm BRD_ID1.R
GPU Power OFF
No GPU Power ON




5	4	3	2	1
D				D
C				C
B				B
A				A

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Title NV_GPU_MEM_FBA[63..32]		
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 Asia Vital Components Co., Ltd.		
Title NV_GPU_MEM DECOUPLING		
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Title NV_GPU_PWR		
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Title NV_GPU_GND		
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Title NV_GPU_DECOUPLING		
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5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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Title NV_GPU_ROM_XTAL_GPU_PLL's		
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<div><div><div></div></div><div>Asia Vital Components Co., Ltd.</div></div>		
TitleNV GPU PWR SRC DETECT		
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 Asia Vital Components Co., Ltd.		
Title GPU_NVVDD_2ph Out		
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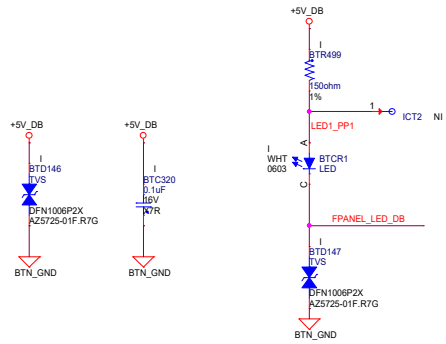
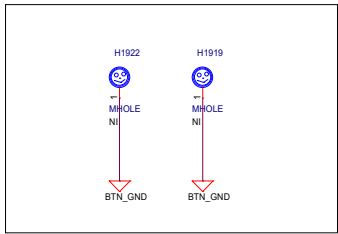
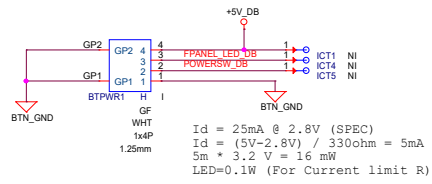
	5	4	3	2	1
D					
C					
B					
A					

 Asia Vital Components Co., Ltd.		
Title RESERVED		
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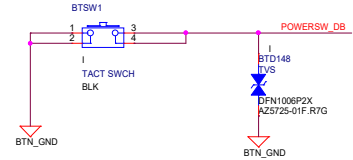
	A	B	C	D	E
1					
2					
3					
4					

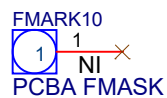
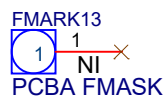
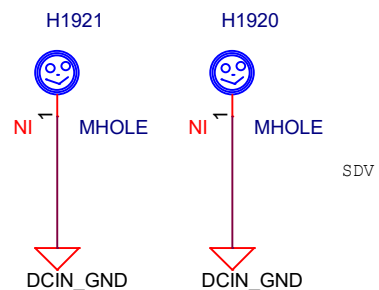
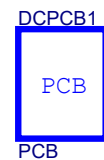
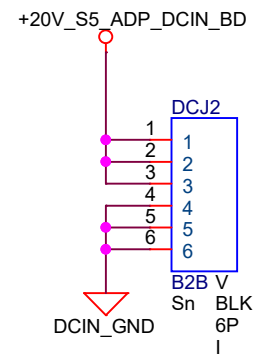
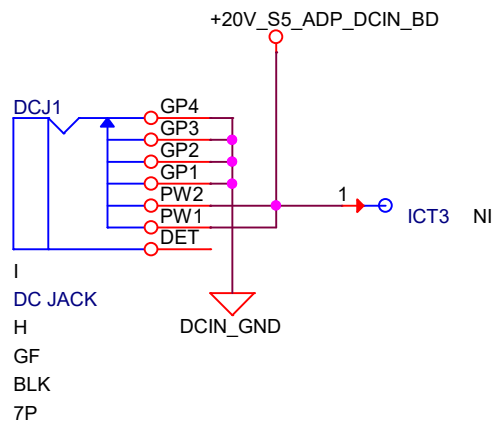
ET2 to SDV

1.VCORE
PR7200 = 130K,PC7218 = 820pF
2. VCCGT
PR7209=137K,PR7216=36.5K,PC7147=820 pF,PR7217=4.02K
3. LV6543BGQW change to LV6543AGQW
4. +1V05 S5(P73) & +1V8 S5(P74) : PL59、PL1105
change to INDUCTOR 1.5uH +/-20% 100KHZ 14A 15mohm SMT
PC7083、PC7089 stuff
+12V S0(P61) : PC108 stuff
5. +VCCSA (P70) : PR7311
change to 7.5Kohm 1% 1/10W 0603
6. PC931 chagne to MLCC 0.01uF 50V +/-10% X7R 0603
Backlight Vout cap add SMD type(PEC3) , PEC86 chagne to no stuff
7. Change VCORE
PR7200 = 130K , PC7218 = 820pF
VCCGT
PR7209=137K , PR7216=36.5K
PC7147=820 pF , PR7217=4.02K
VCCSA
PR12345=10.2K , R7155=82K
PC7246=2.7nF , PC7245=39nF
PR7318=4.02K , Remove PEC67
8. Change
+1V8 S5 (P74)
PC7251、PC7252
Description: MLCC 22uF 6.3V +/-10% X5R 0805
+VCORE (P63)
PFB111、PFB110、PFB109
Description: INDUCTOR 0.33uH +/-20% 100KHZ 19A 5.56mohm SMT
+VCCGT (P64)
PFB93、PFB94
Description: INDUCTOR 0.33uH +/-20% 100KHZ 19A 5.56mohm SMT
9. Change +VCORE (P63)
PL1106、PL1107、PL1108、PL1109
Description: INDUCTOR 0.3uH +/-15% 100KHZ 60A 1.05mohm SMT
+VCCGT (P64)
PL1110、PL1111
Description: INDUCTOR 0.3uH +/-15% 100KHZ 60A 1.05mohm SMT
+VCCSA (P70)
PL2
Description: INDUCTOR 0.36uH +/-15% 100KHZ 50A 1.05mohm SMT
10. Change +5V_S5 (P60)
PR139
R-CHIP 15Kohm 1% 1/16W 0402
PR147
R-CHIP 402ohm 1% 1/16W 0402
PC146
MLCC 560pF 50V +/-10% X7R 0402
+3V3 PWR (P60)
PR153
R-CHIP 20Kohm 1% 1/16W 0402
PR146
R-CHIP 13Kohm 1% 1/16W 0402
PC138
MLCC 560pF 50V +/-10% X7R 040



	S0/S1	S3	S4/S5
LED STATE	ON	BLINKING	OFF





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DC IN			
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